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# A Case Study on VLSI Floor Planning Problem Using Metaheuristic Algorithms

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***Abstract---*** *Floor planning is an essential trouble in very massive scale incorporated-circuit layout automation because it determines the performance, size, yield, and reliability of VLSI chips. From the computational point of view, VLSI floor planning is an NP-hard hassle. Modern very huge scale integration technology is primarily based on constant-define floor plan constraints, normally with an goal of minimizing area and wirelength between the modules. This survey paper gives an up to date account on diverse metaheuristic algorithms used to SOI. As technology advances, circuit sizes and layout complexity in cutting-edge VLSI layout are increasing rapidly. To manage the design complexity, hierarchical design and reuse of IP modules turn out to be popular, which makes floor planning or placement a lot extra crucial than ever [1].*

***Keywords---*** *Metaheuristic Algorithms, Floorplan, Soft Modules, Hard Modules, Simulated Annealing, VLSI.*

## I. FLOOR PLANNING

A floor plan is a square dissection which describes the relative placement of digital modules on the chip. The exponential growth in the size of virtual circuit, reduction in chip size and heterogeneity of circuit factors used in contemporary chips lead to an increase within the complexity of modern digital circuit layout and layout of algorithms [2]. The improvement of integration era has observed the well-known Moore's Law [3].Gordon Moore, the co-founder of Intel, in the 12 months 1965, said that "The variety of transistors per chip would develop exponentially (double each 18 months)". In the design of VLSI (Very Large-Scale Integrated) circuit's floor planning is an crucial section. It determines the topology of format and this hassle is known as VLSI floor planning hassle.

To be NP-tough (Non-deterministic Polynomial-time hard) and it has received plenty attention in latest years. The answer area of the trouble will boom exponentially with the growth of circuits scale, for that reason it is not possible to discover the choicest solution by way of exploring the worldwide answer area [4].

The digital circuit layout trouble is a restricted optimization problem within the combinatorial feel. It is an essential part of the virtual circuit design manner. For a circuit represented by way of internet list, a fixed of modules, its dimensions and a set of pins, the format hassle seeks an assignment of geometric coordinates of the circuit components fulfilling the necessities of the fabrication era (sufficient cord spacing, constrained quantity of wiring layers etc.) at the same time as minimizing positive value criteria. This is accomplished in several tiers along with partitioning, floor planning, placement and routing with each step being a confined optimization problem [5]. Floor planning is an crucial layout step in bodily design of VLSI circuits to plan the positions of a set of circuit modules on a chip for you to optimize the circuit performance.

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The predominant objective of floor planning is to allocate the modules of a circuit right into a chip to optimize a few design metric together with vicinity, twine period and timing. During floor planning the designers have additional flexibility in phrases of length form and orientation of the modules on chip. The shape of the chip and that of the modules is often a rectangle. The representation has a notable effect at the feasibility and complexity of floor plan designs. In this paper details about diverse aspects of floor plan layout problem is given in conjunction with the complete literature survey of VLSI floor planning hassle.

Very huge-scale included floor plan is to set up the modules on a chip and the given inputs of the location hassle is a hard and fast of blocks defined as B = B1, B2, ….Bn. Each block Bi is square with fixed orientation and a tuple (wi, hello), wherein wi is defined because the width and hi is described because the peak. There are two different kinds of modules:

1. Hard module. The difficult module's shape is fixed, and is denoted as (W, H), where W is the width and H is the height of the module.

2. Soft module. Soft module's region is likewise fixed, but the ratio of width/top is protected in a given range. It may be denoted as (S, L, U), wherein S represents the area, L and U the lower and higher boundary of the width/height ratio. In case that the modules are given, the objective of VLSI floorplanning is to set up the modules on a chip below the restrictions that any modules aren't overlapped, and the place, cord period and other performance indices are top-quality [4].

There are layout systems in floorplan, particularly, cutting and non-cutting floorplan. A cutting floorplan can be received by way of repetitively slicing the floorplan horizontally or vertically, whereas a non-reducing floorplan can not [6]. The given size of each tough module should be kept. All modules are free of rotation; if a module is turned around, its width and height are exchanged. Figure 1 shows a slicing floorplan. A cutting tree is used to symbolize a slicing floorplan; it's miles a binary tree with modules at the leaves and reduce sorts on the inner nodes. There are two cut types, H and V. The H cut divides the floorplan horizontally, and the left (right) infant represents the lowest (pinnacle) sub-floorplan. In Similar way, the V cut divides the floorplan vertically, and the left (proper) baby represents the left (proper) sub-floorplan.

The non-reducing floorplan is more fashionable than the cutting floorplan as shown in Figure 2. However, because of its non-slicing shape, reducing tree cannot be used to version it.

Instead, we will use a horizontal constraint graph (HCG) and a vertical constraint graph (VCG) to model a non-cutting floorplan.

To practice any optimization method for floorplan design, we need to first encode a floorplan as an answer that is known as a floorplan representation. A floorplan illustration now not only induces an answer space that contains all feasible answers described through the representation but also induces a unique solution shape that guides the quest of the optimization method to discover a favored floorplan in the answer space. Most popular floorplan

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representations are Normalized Polish Expression, B*-tree, Sequence Pair, O-tree. Details about numerous floorplan representations which have been used for VLSI floorplanning can be visible in [7].

The aim of floorplanning is to optimize a predefined price feature, along with the place of a ensuing floorplan given through the minimal bounding rectangle of the floorplan area. Chip silicon value immediately correlates to the floorplan region. Chip silicon value can be high if the area is large. The space within the floorplan bounding rectangle exposed by way of any module is called white area or dead area. Other floorplanning fee, along with wirelength, may also be considered. Shorter wirelength not only can reduce signal delay however also can facilitate wire interconnection on the routing level. So the objective of floorplanning also can be a blended cost, a aggregate of vicinity plus wire length.

Increasing design complexity and new circuit homes and requirements have reshaped the contemporary floorplanning trouble. The new concerns and challenges make the trouble much greater hard. Two such important considerations are following:-Unlike tough modules with fixed heights and widths, smooth modules can change their heights and widths while preserving the identical module location. The issue ratio bounds are given as inputs for each module. There are many strategies for the adjustment of smooth-module dimensions.

Modern VLSI design is usually based totally on a fixed-die (fixed-define) floorplan [8], in preference to a variable-die floorplan. A floorplan with pure location minimization with none fixed-outline constraints may be useless, because it can't healthy into the given outline. The classical floorplanning commonly handles best module packing to reduce silicon vicinity, not like it the contemporary floorplanning ought to be formulated as fixed-define floorplanning

In the context of circuit design, floorplanning is the method of putting circuit modules of arbitrary sizes and dimensions on a given layout vicinity with an objective of minimizing area and wirelength between the modules and this trouble has been solved via using diverse iterative approaches in literature [9]. They search for an progressed floorplan by using making neighborhood adjustments till a feasible floorplan is received or no extra enhancements may be received. A exact literature evaluate of the popular metaheuristic algorithms which have been used to address VLSI floorplanning problem is given beneath. It is one of the most famous strategies for floorplan optimization. To follow simulated annealing for floorplan design, first off floorplan is encoded as an answer, known as a floorplan representation, which fashions the geometric relation of modules in a floorplan. This floorplan representation not only induces a solution space that includes all possible answers described by way of the illustration however additionally induces a unique solution structure that courses the quest of simulated annealing to discover a desired floorplan within the answer area ([10], [11]).

D. F. Wong and C. L. Liu (1989) [12] used polish expressions to symbolize floorplans and employ the hunt technique of simulated annealing. They used simulated annealing for the case where all modules are rectangular and reduce place and interconnection wirelength.

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Koji kiyota, Kunihiro fuiiyoshi (2000) [13] proposed a novel solution space of floorplans for simulated annealing (SA) which includes the all preferred floorplans with actual n rooms, where n is the wide variety of given modules, the usage of series pair.

Chen, T.C., Chang (2006) [14] have studied types of cutting-edge floorplanning issues: 1) constant-outline floorplanning and 2) bus-driven floorplanning (BDF). This floor planner makes use of B*- tree floorplan illustration based totally on rapid 3-level simulated annealing (SA) scheme known as Fast-SA.

Fang, J.P., Chang, Y.L, et. Al. (2009) [15] followed a parallel computing environment to increase the throughput of answer space searching in order to cope with the floorplan layout with extensive amount of interconnections and design blocks.

S. Anand , S. Saravanasankar (2010) [16] the purpose of their work become to decrease the unused vicinity, this is, lifeless space within the floorplan, further to those goals. They evolved a Simulated Annealing Algorithm (SAA) based heuristic, namely Simulated Spheroidizing Annealing Algorithm (SSAA) and upgrades inside the proposed heuristic set of rules are also suggested to improve its overall performance.

Jianli Chen, Wenxing Zhu (2011) [17] offered a hybrid simulated annealing algorithm (HSA) for nonslicing VLSI floorplanning. They used a brand new grasping approach to construct an initial B*-tree, a brand new operation on the B*-tree to explore the hunt area.

## II. GENETIC ALGORITHM (GA)

It is a worldwide seeks method stimulated with the aid of evolution. The crux of GA lies inside the “survival of the fittest” strategy. The input to GA is a fixed of random people, termed as the initial populace. Each man or woman in the population is a chromosome that represents a strategy to the given hassle in an encoded shape. Using nicely-described genetic operators, GA evolves the individuals in the population generation through technology until an surest or near to most beneficial answer is located. The health of the people is evaluated in a health function.

B. Gwee and M. Lim (1999) [18] described a genetic algorithm with heuristic-based format decoder (GAHD) for floorplanning in IC design which use GA to search for an most suitable arrangement of circuit modules on a pre-certain format area.

Ning Xu, Feng Huang et. Al. (2006) [19] proposed a multithread scheme for parallelizing a genetic set of rules for BBL placement optimization. The parallel genetic algorithms (PGA) are found out, using sequence-pair (SP) because the illustration so that you can both speed up a trouble or to achieve a higher accuracy of answers to a problem.

Maolin Tang and Xin Yao (2007) [20] proposed a memetic set of rules (MA) for a nonslicing and tough-module VLSI floorplanning hassle. This MA is a hybrid genetic algorithm that uses an effective genetic seek technique to explore the hunt area and an efficient nearby seek technique to make the most information within the seek area.

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Pradeep Fernando and Srinivas Katkoori (2008) [21] proposed a multi-objective genetic set of rules for floorplanning that concurrently minimizes region and overall wirelength. The proposed genetic floor planner is the first to use non-domination ideas to rank answers. Samsuddin et. Al. (2008) [22] proposes an optimization technique for macro-cell placement which minimizes the chip region length. The binary tree method for non-reducing tree construction system is utilized for the position and location optimization of macro-cell format in very large scaled included (VLSI) design.

Various styles of genetic algorithms: simple genetic set of rules (SGA), steady-country algorithm (SSGA) and adaptive genetic algorithm (AGA) are employed so that it will look at their performances in converging to their global minimums. Jianli Chen, Wenxing Zhu (2010) [23] defined that hybrid genetic algorithm (HGA) uses an effective genetic search technique to discover the hunt space and an efficient nearby seek approach to make the most records inside the seek vicinity. Gracia Nirmala Rani, Rajaram.S et. Al. (2012) [24] provided a Genetic (GA) algorithm based totally thermal-aware floorplanning framework. Primary objective for floorplanning is to decrease the whole vicinity required to deal with all the purposeful blocks on a chip and also to lessen excessive temperature and to distribute temperature evenly across a chip in an framework. B*tree representations with Genetic (GA) algorithm is used to calculate floorplanning temperature based on the strength dissipation.

## III. PARTICLE SWARM OPTIMIZATION (PSO)

It is an optimization method stimulated by swarm intelligence and concept in well known consisting of bird flocking or even human social conduct. PSO is a population-primarily based evolutionary algorithm wherein the set of rules is initialized with a population of random answers. However, unlike maximum of other populace-based totally evolutionary algorithms, Particle swarm optimization is motivated by using the simulation of social conduct in preference to the survival of the health.

Guolong Chen et. Al. (2008) [25] proposed a singular floorplanning set of rules primarily based on Discrete PSO (DPSO) algorithm, in which integer coding based on module variety turned into adopted and the ideas of mutation and crossover operator inside the Genetic Algorithm (GA) are also integrated into the proposed PSO set of rules to achieve better range and smash away from neighborhood optima.

Zhen Chen et. Al. (2012) [26] proposed a co evolutionary multi goal particle swarm optimization (CMOPSO)algorithm to solve a VLSI Floorplanning hassle which is a multi-goal combinatorial optimization and has been proved to be a NP-tough problem.

Ant colony optimization (ACO) is a population primarily based metaheuristic that can be used to discover premiere method to tough optimization problems. One of the maximum intensively studied troubles in the area of optimization is travelling salesman hassle (TSP). The visiting salesman trouble is a hassle in combinational optimization. It is a NP-hard trouble.

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The ant-based totally metaheuristic set of rules consists of 3 ranges, that are the initialization, the construction and the comments. The primary stage i.E. Initialization level involves the parameters settings inclusive of the number of colonies and the range of ants. The next stage i.E. Production level includes the construction of direction on the idea of pheromone attention. The closing one i.E. The feedback stage offers with the extraction and the reinforcement of the ants journeying reports obtained all through the previous looking direction.

Chyi-Shiang Hoo et. Al. (2013) [27] proposed a new floorplanner, specifically Variable-Order Ant System (VOAS) is proposed to address VLSI floorplanning design. VOAS transforms parameter ˇ in Ant System (AS) to a variable and those various nearby and worldwide elements enable the ant to make the nice feasible desire. Experimental effects by the use of MCNC and GSRC benchmark circuits display that VOAS offers advanced effects in phrases of region and composited function of location and twine period, in comparison to different latest and current floorplanning/placement algorithms.

## IV. CONCLUSION AND FUTURE ENHANCEMENT

In the context of circuit layout, floorplanning is the process of placing circuit modules of arbitrary sizes and dimensions on a given layout vicinity and it gives answer to the exclusive questions of VLSI layout which include form of modules and vicinity of modules. The primary goal of floorplanning is to allocate the modules of a circuit into a chip to optimize a few design metric which includes place, twine length and timing. Optimized VLSI floorplan designs will enhance the overall performance and size of VLSI chips. It will also be beneficial in figuring out the yield and reliability of VLSI chips.

For cutting-edge floorplan designs, some other extension may be to paintings with rectilinear modules (as an instance, T-fashioned or L-fashioned modules). That may be achieved via splitting these rectilinear shapes into rectangles and editing the placing set of rules to keep the ones corresponding rectangles compacted. As era advances, the number of modules in a chip becomes massive, in an effort to deal with the scalability hassle successfully and successfully, hierarchical floorplanning also can be used. The hierarchical approach recursively divides a floorplan vicinity into a set of sub-areas and solves the ones sub-troubles independently.

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## REFERENCES

[1] Tamilselvi, N., Krishnamoorthy, P., Dhamotharan, R., Arumugam, P., & Sagadevan, E. (2012). Analysis of total phenols, total tannins and screening of phytocomponents in Indigofera aspalathoides (Shivanar Vembu) Vahl EX DC. *Journal of Chemical and Pharmaceutical Research*, *4*(6), 3259-3262.

[2] Abraham, A.G., Manikandan, A., Manikandan, E., Jaganathan, S.K., Baykal, A., & Renganathan, P. (2017). Enhanced opto-magneto properties of Ni x Mg1–x Fe2O4 (0.0≤ x≤ 1.0) ferrites nano-catalysts. *Journal of Nanoelectronics and Optoelectronics*, *12*(12), 1326-1333.

[3] Barathiraja, C., Manikandan, A., Mohideen, A.U., Jayasree, S., & Antony, S.A. (2016). Magnetically recyclable spinel Mn x Ni 1− x Fe 2 O 4 (x=0.0–0.5) nano-photocatalysts: structural, morphological and opto-magnetic properties. *Journal of Superconductivity and Novel Magnetism*, *29*(2), 477-486.

[4] Kaviyarasu, K., Manikandan, E., Nuru, Z.Y., & Maaza, M. (2015). Investigation on the structural properties of CeO2 nanofibers via CTAB surfactant. *Materials Letters*, *160*, 61-63.

[5] Kaviyarasu, K., Manikandan, E., & Maaza, M. (2015). Synthesis of CdS flower-like hierarchical microspheres as electrode material for electrochemical performance. *Journal of Alloys and Compounds*, *648*, 559-563.

[6] Sachithanantham, P., Sankaran, S., & Elavenil, S. (2015). Experimental study on the effect of rise on shallow funicular concrete shells over square ground plan. *International Journal of Applied Engineering Research*, *10*(20), 41340-41345.

[7] Jayalakshmi, T., Krishnamoorthy, P., Ramesh Kumar, G., &Sivaman, I.P. (2011). Optimization of culture conditions for keratinase production in Streptomyces sp. JRS19 for chick feather wastes degradation, *Journal of Chemical and Pharmaceutical Research*, *3*(4), 498-503.

[8] Kumarave, A., & Rangarajan, K. (2013). Routing alogrithm over semi-regular tessellations. In *2013 IEEE Conference on Information & Communication Technologies*, 1180-1184.

[9] Sonia, M.M.L., Anand, S., Vinosel, V.M., Janifer, M.A., Pauline, S., & Manikandan, A. (2018). Effect of lattice strain on structure, morphology and magneto-dielectric properties of spinel NiGdxFe2− xO4 ferrite nano-crystallites synthesized by sol-gel route. *Journal of Magnetism and Magnetic Materials*, *466*, 238-251.

[10] Rebecca, L.J., Susithra, G., Sharmila, S., & Das, M.P. (2013). Isolation and screening of chitinase producing Serratia marcescens from soil. *Journal of Chemical and Pharmaceutical Research*, *5*(2), 192-195.

[11] Banumathi, B., Vaseeharan, B., Rajasekar, P., Prabhu, N.M., Ramasamy, P., Murugan, K., & Benelli, G. (2017). Exploitation of chemical, herbal and nanoformulated acaricides to control the cattle tick, Rhipicephalus (Boophilus) microplus–a review. *Veterinary parasitology*, *244*, 102-110.

[12] Gopinath, S., Sundararaj, M., Elangovan, S., & Rathakrishnan, E. (2015). Mixing characteristics of elliptical and rectangular subsonic jets with swirling co-flow. *International Journal of Turbo & Jet-Engines*, *32*(1), 73-83.

[13] Thooyamani, K.P., Khanaa, V., & Udayakumar, R. (2014). Efficiently measuring denial of service attacks using appropriate metrics. *Middle - East Journal of Scientific Research*, *20*(12): 2464-2470.

[14] Padmapriya, G., Manikandan, A., Krishnasamy, V., Jaganathan, S.K., & Antony, S.A. (2016). Enhanced Catalytic Activity and Magnetic Properties of Spinel MnxZn1−xFe2O4 (0.0 ≤ x ≤ 1.0) Nano-Photocatalysts by Microwave Irradiation Route. *Journal of Superconductivity and Novel Magnetism*, *29*(8): 2141-2149.

[15] Rajesh, E., Sankari, L.S., Malathi, L., & Krupaa, J.R. (2015). Naturally occurring products in cancer therapy. *Journal of pharmacy & bioallied sciences*, *7*(1), S181-S183.

[16] Vanangamudi, S., Prabhakar, S., Thamotharan, C., & Anbazhagan, R. (2014). Dual fuel hybrid bike. *Middle-East Journal of Scientific Research*, *20*(12): 1819-1822.

[17] Brindha, G., Krishnakumar, T., & Vijayalatha, S. (2015). Emerging trends in tele-medicine in rural healthcare. *International Journal of Pharmacy and Technology*, *7*(2): 8986-8991.

[18] Sharmila, S., Rebecca, L.J., Chandran, P.N., Kowsalya, E., Dutta, H., Ray, S., & Kripanand, N.R. (2015). Extraction of biofuel from seaweed and analyse its engine performance. *International Journal of Pharmacy and Technology*, *7*(2), 8870-8875.

[19] Thooyamani, K.P., Khanaa, V., & Udayakumar, R. (2014). Using integrated circuits with low power multi bit flip-flops in different approch. *Middle-East Journal of Scientific Research*, *20*(12): 2586-2593.

[20] Thooyamani, K.P., Khanaa, V., & Udayakumar, R. (2014). Virtual instrumentation based process of agriculture by automation. *Middle-East Journal of Scientific Research*, *20*(12): 2604-2612.

[21] Udayakumar, R., Kaliyamurthie, K.P., & Khanaa, T.K. (2014). Data mining a boon: Predictive system for university topper women in academia. *World Applied Sciences Journal*, *29*(14): 86-90.

[22] Anbuselvi, S., Rebecca, L.J., Kumar, M.S., & Senthilvelan, T. (2012). GC-MS study of phytochemicals in black gram using two different organic manures. *J Chem Pharm Res*., *4*, 1246-1250.

[23] Subramanian, A.P., Jaganathan, S.K., Manikandan, A., Pandiaraj, K.N., Gomathi, N., & Supriyanto, E. (2016). Recent trends in nano-based drug delivery systems for efficient delivery of phytochemicals in chemotherapy. *RSC Advances*, *6*(54), 48294-48314.

[24] Thooyamani, K.P., Khanaa, V., & Udayakumar, R. (2014). Partial encryption and partial inference control based disclosure in effective cost cloud. *Middle-East Journal of Scientific Research*, *20*(12): 2456-2459.

[25] Lingeswaran, K., Prasad Karamcheti, S.S., Gopikrishnan, M., & Ramu, G. (2014). Preparation and characterization of chemical bath deposited cds thin film for solar cell. *Middle-East Journal of Scientific Research*, *20*(7), 812-814.

[26] Maruthamani, D., Vadivel, S., Kumaravel, M., Saravanakumar, B., Paul, B., Dhar, S.S., & Ramadoss, G. (2017). Fine cutting edge shaped Bi2O3rods/reduced graphene oxide (RGO) composite for supercapacitor and visible-light photocatalytic applications. *Journal of colloid and interface science*, *498*, 449-459.

[27] Gopalakrishnan, K., SundeepAanand, J., & Udayakumar, R. (2014). Electrical properties of doped azopolyester. *Middle-East Journal of Scientific Research*, *20*(11), 1402-1412.

[28] Subhashree, A.R., Parameaswari, P.J., Shanthi, B., Revathy, C., & Parijatham, B.O. (2012). The reference intervals for the haematological parameters in healthy adult population of chennai, southern India. *Journal of Clinical and Diagnostic Research: JCDR*, *6*(10), 1675-1680.

[29] Niranjan, U., Subramanyam, R.B.V., & Khanaa, V. (2010). Developing a web recommendation system based on closed sequential patterns. *International Conference on Advances in Information and Communication Technologies*, 171-179.

[30] Slimani, Y., Baykal, A., & Manikandan, A. (2018). Effect of Cr3+ substitution on AC susceptibility of Ba hexaferrite nanoparticles. *Journal of Magnetism and Magnetic Materials*, *458*, 204-212.

[31] Premkumar, S., Ramu, G., Gunasekaran, S., & Baskar, D. (2014). Solar industrial process heating associated with thermal energy storage for feed water heating. *Middle East Journal of Scientific Research*, *20*(11), 1686-1688.

[32] Kumar, S.S., Karrunakaran, C.M., Rao, M.R.K., & Balasubramanian, M.P. (2011). Inhibitory effects of Indigofera aspalathoides on 20-methylcholanthrene-induced chemical carcinogenesis in rats. *Journal of carcinogenesis*, *10*, 2011.

[33] Beula Devamalar, P.M., Thulasi Bai, V., & Srivatsa, S.K. (2009). Design and architecture of real time web-centric tele health diabetes diagnosis expert system. *International Journal of Medical Engineering and Informatics*, *1*(3), 307-317.

[34] Ravichandran, A.T., Srinivas, J., Karthick, R., Manikandan, A., & Baykal, A. (2018). Facile combustion synthesis, structural, morphological, optical and antibacterial studies of Bi1− xAlxFeO3 ($0.0 \leq x \leq 0.15$) nanoparticles. *Ceramics International*, *44*(11), 13247-13252.

[35] Thovhogi, N., Park, E., Manikandan, E., Maaza, M., & Gurib-Fakim, A. (2016). Physical properties of CdO nanoparticles synthesized by green chemistry via Hibiscus Sabdariffa flower extract. *Journal of Alloys and Compounds*, *655*, 314-320.

[36] Thooyamani, K.P., Khanaa, V., & Udayakumar, R. (2014). Wide area wireless networks-IETF. *Middle-East Journal of Scientific Research*, *20*(12), 2042-2046.

[37] Sundar Raj, M., Saravanan, T., & Srinivasan, V. (1785). Design of silicon-carbide based cascaded multilevel inverter. *Middle-East Journal of Scientific Research*, *20*(12), 1785-1791.

[38] Achudhan, M., & Prem Jayakumar, M. (2014). Mathematical modeling and control of an electrically-heated catalyst. *International Journal of Applied Engineering Research*, *9*(23).

[39] Thooyamani, K.P., Khanaa, V., & Udayakumar, R. (2013). Application of pattern recognition for farsi license plate recognition. *Middle-East Journal of Scientific Research*, *18*(12), 1768-1774, 2013.

[40] Jebaraj, S., & Iniyan S. (2006). Renewable energy programmes in India. *International Journal of Global Energy*, 26: 232-257.

[41] Pawale, P.V., & Puranik, V.G. (2014).Distributed Node Connectivity Improving & Monitoring Mechanism for WSN. *International Scientific Journal on Science Engineering & Technology*, *17*(11), 1017-1025.

[42] K. Prabavathy& Dr. P. Sumathi, (2013). Text Mining Interpreting Knowledge Discovery from Biomed Articles. *The SIJ Transactions on Advances in Space Research & Earth Exploration*, *1*(2), 5-8.

[43] Arora, S., Kaur, P., & Arora, P. (2013). Economical Maintenance and Replacement Decision Making in Fleet Management using Data Mining. *The SIJ Transactions on Advances in Space Research & Earth Exploration, 1*(2), 9-20.

[44] Dr. Malhotra, R., & Jain, P. (2013). Novel Testing Tools for a Cloud Computing Environment- A Review. *The SIJ Transactions on Advances in Space Research & Earth Exploration, 1*(3), 25-29.

[45] Dr. Malhotra, R., & Jain, P.(2013). Testing Techniques and its Challenges in a Cloud Computing Environment. *The SIJ Transactions on Advances in Space Research & Earth Exploration, 1*(3), 30-35.

[46] Gowtham, S., & Karuppusamy, S. (2019). Review of Data Mining Classification Techniques. *Bonfring International Journal of Software Engineering and Soft Computing, 9*(2), 8-11.

[47] Dev, P., Syiemiong, J.V., Iawphniaw, O., & Bhutia, R.D., (2019). IOT Based Accident Preventing and Reporting System. *Bonfring International Journal of Software Engineering and Soft Computing, 9*(2), 12-15.

[48] Raguman, R., Santhakumar, M., Thomas, X.P., & Revathi, M. (2019). 3D Adventure Game Using Unity. *Bonfring International Journal of Software Engineering and Soft Computing, 9*(2), 16-20.

[49] Baskaran, S., Sowmiya, P., Umme Salma, I., & Vaitheeshwari, R., Dr. Baskaran, S., Sowmiya, P., Umme Salma, I., & Vaitheeshwari, R. (2017).Implementation of Wi-Fi and VLC towards 5G. *The SIJ Transactions on Computer Networks & Communication Engineering (CNCE), 5*(6), 6-10.

[50] Agarwal, A.(2018).Protocol Architecture of LTE Release 12.*The SIJ Transactions on Computer Networks & Communication Engineering (CNCE), 6*(1), 1-9.

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