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NETWORK INTRUSION DETECTION SYSTEM USING MODIFIED BLOOM FILTER

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ABSTRACT

This paper presents an efficient implementation of the commonly used hash algorithm self-postulated in a modified bloom filter along with the details of standard bloom filter, with the counter bloom filter implementation. We have extended the report with a way of improvising the bloom filter in the network layer so that the threats are blocked in the network as well as to make the network safer.

A Bloom filter is a simple space-efficient randomized data structure for representing a set in order to support membership queries. Bloom filters allow false positives but the space savings often outweigh this drawback when the probability of an error is controlled. In this paper, we the architectural benefits of hybridizing the filter is clearly given, along with the way to construct it in an efficient manner. By future applications we mainly mean Network based intrusion detectors, which can help in controlling the advanced forms of intrusions threat detection. The aim of this report is to survey the ways in which Bloom filters have been used and modified in a variety of network problems, with the aim of providing a unified mathematical and practical framework for understanding them and stimulating their use in future applications.

Keywords: *Bloom Filter, Network Intrusion Detection System.*

INTRODUCTION

An intrusion detection system (IDS) is a device or software application that monitors network or system activities for malicious activities or policy violations and produces reports to a Management Station. Some systems may attempt to stop an intrusion attempt but this is neither required nor expected of a monitoring system. Intrusion detection and prevention systems (IDPS) are primarily focused on identifying possible incidents, logging Information about them, and reporting attempts.

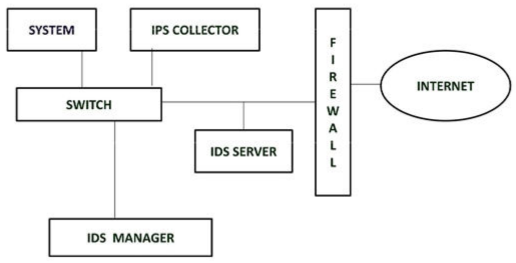


Fig 1: Intrusion Detection System

Comparison of NIDS with Firewalls: Though they both relate to network security, a network intrusion detection system (NIDS) differs from a firewall in that a firewall looks outwardly for intrusions in order to stop them from happening. Firewalls limit access between networks to prevent intrusion and do not signal an attack from inside the network. An NIDS evaluates a suspected intrusion once it has taken place and signals an alarm. An NIDS also watches for attacks that originate from within a system. This is traditionally achieved by examining network communications, identifying heuristics and patterns (often known as signatures) of common computer attacks, and taking action to alert operators. A system that terminates connections is called an intrusion prevention system, and is another form of an application layer firewall. (Vasanthy and Jeganathan 2007, Vasanthy et.al., 2008, Raajasubramanian et.al., 2011, Jeganathan et.al., 2012, 2014, Sridhar et.al., 2012, Gunaselvi et.al., 2014, Premalatha et.al., 2015, Seshadri et.al., 2015, Shakila et.al., 2015, Ashok et.al., 2016, Satheesh Kumar et.al., 2016).

LITERATURE SURVEY

It has proposed a system here, which is a hardware-implementable pattern matching algorithm for content filtering applications, which is scalable in terms of speed, the number of patterns and the pattern length [1]. The algorithm spoken about in this paper is based on a memory efficient multi-hashing data structure called Bloom filter. Embedded on-chip memory blocks in FPGA/VLSI chips are used to construct Bloom filters which can suppress a large fraction of memory accesses and speed up string matching. It has presented hardware architecture for highly efficient intrusion detection systems. By moving both the string matching and the linking of multi-part rules to hardware, their architecture leaves the host system free for higher-level analysis [2]. The tool automates the creation of efficient Field Programmable Gate Array architectures (FPGA). The generated hardware allows an FPGA based system to perform deep-packet inspection of streams at up to 10 Gb/s line rates at a high level of area efficiency. It have introduced a technique, based on a tree-based content addressable memory structure, for a pattern matching engine for use in a hardware-based network intrusion detection system. This technique involves hardware sharing at bit level in order to exploit powerful logic optimizations for multiple strings represented as a Boolean expression [3]. Their approach has been used to implement the entire SNORT rule set with around 12% of the area on a Xilinx XC2V8000

FPGA. The design can run at a rate of approximately 2.5 Gigabits per second, and is approximately 30% smaller in area when compared with published results. In this paper introduces the concept of using internal sensors to perform intrusion detection in computer systems.At a practical level, direct monitoring can be implemented using external or internal sensors. Internal sensors provide advantages with respect to reliability, completeness, timeliness and volume of data, in addition to efficiency and resistance against attacks. This paper introduces a concept of embedded detectors as a mechanism for localized data reduction [4]. Their implementation shows that it is possible to build both specific and generic detectors. Detection testing shows that embedded detectors have the capability of detecting a significant percentage of new attacks. It has proposed a Network Intrusion Detection System (NIDS) embedded in a Smart Sensor inspired device, under a Service Oriented Architecture (SOA) approach, able to operate independently as an anomaly-based NIDS or integrated, transparently, in a Distributed Intrusion Detection System (DIDS). The main goal of the work is to reduce the huge volume of management tasks inherent to this type of network services, as well as facilitating the design of DIDS whose managing complexity could be restricted within well-defined margins [5]. It has coined an FPGA-based implementation of the Bloom filter virus detection code that is compiled from the native C to VHDL and mapped onto a Virtex XC2V8000 FPGA is described in this paper [9]. Their results show that a single engine tailored for handling virus signatures of length eight bytes can achieve a throughput of 18.6 Gbps while occupying only 8% of the FPGA area. It has introduced A k-stage pipelined Bloom filter architecture to decrease power consumption. Pipelined Bloom filter architecture decreases power consumption in comparison to the standard Bloom filter [10]. The 4-stage pipelined Bloom filter is more appropriate than standard Bloom filter when the power consumption is critical. (Manikandan et.al., 2016, Sethuraman et.al., 2016, Senthil Thambi et.al., 2016, Ashok et.al., 2018, Senthilkumar et.al., 2018,).

EXISTING SYSTEM

Standard Bloom Filter: Unlike sets based on hash tables, any Bloom filter can represent the entire universe of elements. In this case, all bits are 1. Another consequence of this property is that add never fails due to the data structure "filling up." However, the false positive rate increases steadily as elements are added until all bits in the filter are set to 1, so a negative value is never returned. At this point, the Bloom filter completely ceases to differentiate between differing inputs, and is functionally useless.

Parallel Bloom Filter: The parallel bloom filters carry out the whole operation of the bloom filter in a parallel fashion in order in perform faster and efficiently. The parallel bloom filter is the basis of many other bloom filters.

Pipelined Bloom Filter: By fully pipelined, it is meant that each stage has only one hash function unlike the two-stage version where there are many hash functions per stage. The fully pipelined Bloom filter has the same number of hash functions as the regular Bloom filter. Hence, the false positive probability is the same. In the query phase, the first hash function, h1, is fed by a new query string every cycle. A query string is progressed to the next stage only when the previous hash function produces a match (i.e., lookup value, LVi=1). The programming phase is the same as the regular Bloom filter.

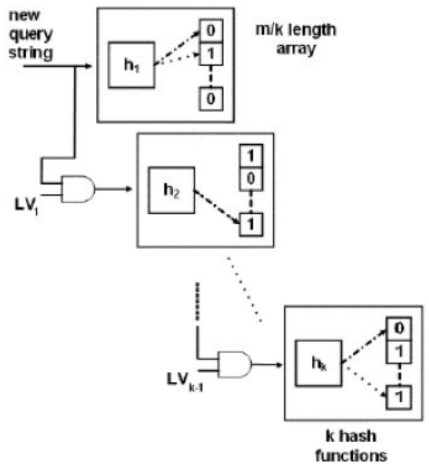


Fig 1: Hardware implementation for the fully pipelined Bloom filter Architecture

PROPOSED SYSTEM

Modified Bloom Filter: Deleting elements from a Bloom filter cannot be done simply by changing ones back to zeros, as a single bit may correspond to multiple elements. To allow for deletions, a counting Bloom filter (CBF) uses an array of n counters instead of bits; the counters track the number of elements currently hashed to that location. Deletions can now be safely done by decrementing the relevant counters. A standard Bloom filter can be derived from a counting Bloom filter by setting all non-zero counts to 1. Counters must be chosen large enough to avoid overflow; for most applications, four bits suffice. We generally use the rule of four bits per counter when comparing results of our data structure with a standard CBF, although we do note that this could be reduced somewhat with some additional complexity. A CBF obtains space savings by allowing false positives.

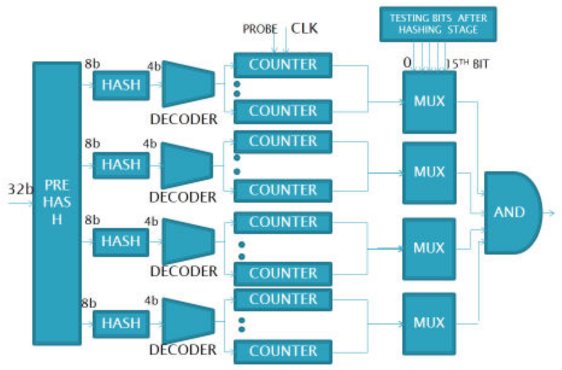


Fig 2: Architecture for Single Pattern Matching Algorithm

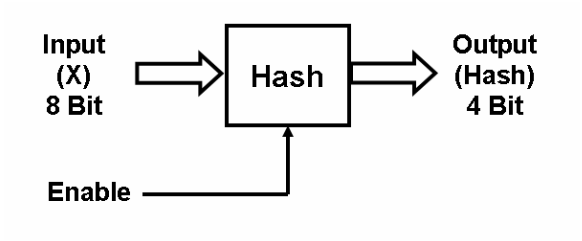
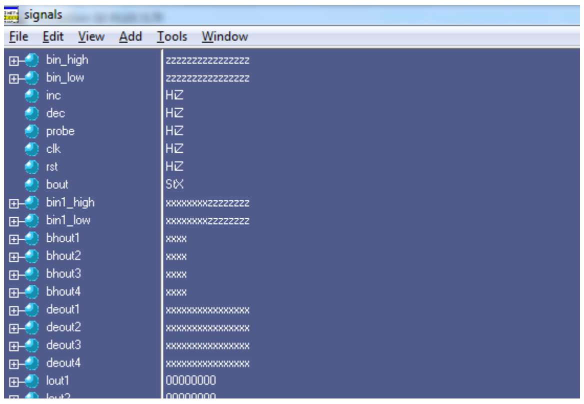


Fig 3: Hash Function Block

Software Analysis: There are two softwares used to the extents for analyzing the data and output in terms of different simulation. ModelSim V5.7 has been mainly used to simulate the output of the software and its output shows a rather good consistency. The modelsim simulations are shown in the result screen shots. The next software used to a larger brief extent is XilinxISE V9.2, Xilinx is a consistent software to perform design implementation and power analysis in such cases of Verilog or VHDL simulation. Xilinx is also a code generating and forging software for the VLSI design kits such as SPARTAN, VERTEX etc.



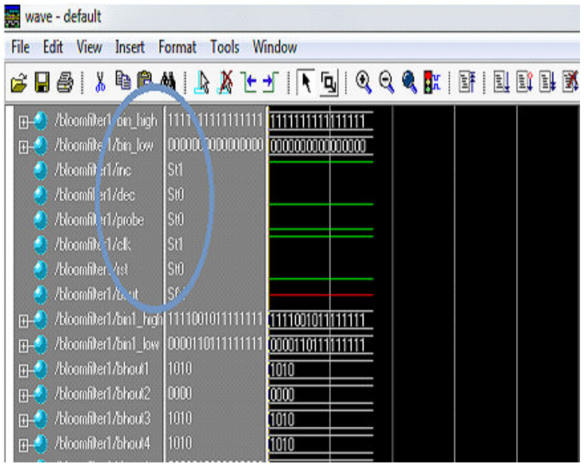
```
bin_high   zzzzzzzzzzzzzzzz
bin_low    zzzzzzzzzzzzzzzz
inc        HiZ
dec        HiZ
probe      HiZ
clk        HiZ
rst        HiZ
bout       StX
bin1_high  xxxxxxxxzzzzzzzz
bin1_low   xxxxxxxxzzzzzzzz
bhout1     xxxx
bhout2     xxxx
bhout3     xxxx
bhout4     xxxx
deout1     xxxxxxxxxxxxxxxx
deout2     xxxxxxxxxxxxxxxx
deout3     xxxxxxxxxxxxxxxx
deout4     xxxxxxxxxxxxxxxx
lout1      00000000
```

Fig 4: Signal Input for the functions

RESULTS AND DISCUSSION

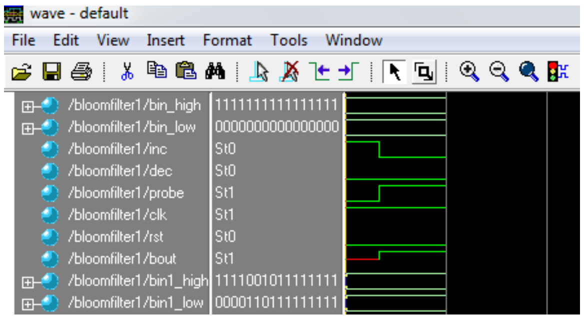
Behavioral Simulation: The above shown figure is a Signal feed dock of ModelSim V5.7 for the Modified bloom filter. The inputs in the above are "bin_low, bin_high", along with the inputs, We use four control triggers Probe, Increment, decrement and clock. Based on the above changes we control the dataflow of the bloom filter. This Bloom filter is a database with reduced string size. The Increment and decrement value is for the control of Up/Down counter whereas the clock is the cyclic inputs, and the value of Probe is to control between the two phases of testing and programming. This would be clearly explained in the below shown simulation and tabulations. There are two phases in the bloom filters output. The first part of the result can be said to as to insertion phase, where the database is created by adding n-number of enteries to the up counters.

The bloom filter takes all these enteries in a encrypted form. The database is a set of hashed hexadecimal bits which are later converged into a very low memory consuming structure.



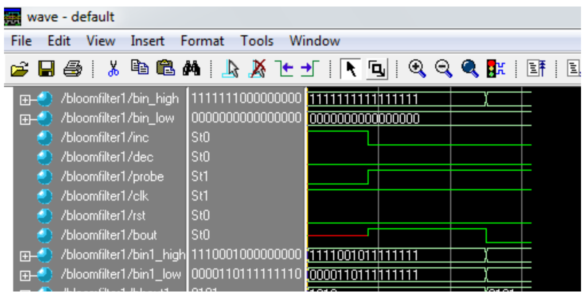
```
/bloomfilter1/bin_high   1111111111111111
/bloomfilter1/bin_low    0000000000000000
/bloomfilter1/inc        St1
/bloomfilter1/dec        St0
/bloomfilter1/probe      St0
/bloomfilter1/clk        St1
/bloomfilter1/rst        St0
/bloomfilter1/bout       [illegible]
/bloomfilter1/bin1_high  1111001011111111
/bloomfilter1/bin1_low   0000110111111111
/bloomfilter1/bhout1     1010
/bloomfilter1/bhout2     0000
/bloomfilter1/bhout3     1010
/bloomfilter1/bhout4     1010
```

Fig 5: The Output for the insertion of the bit.



```
/bloomfilter1/bin_high   1111111111111111
/bloomfilter1/bin_low    0000000000000000
/bloomfilter1/inc        St0
/bloomfilter1/dec        St0
/bloomfilter1/probe      St1
/bloomfilter1/clk        St1
/bloomfilter1/rst        St0
/bloomfilter1/bout       St1
/bloomfilter1/bin1_high  1111001011111111
/bloomfilter1/bin1_low   0000110111111111
```

Fig 6: The output of the testing bits



```
/bloomfilter1/bin_high   1111111000000000  1111111111111111
/bloomfilter1/bin_low    0000000000000000  0000000000000000
/bloomfilter1/inc        St0
/bloomfilter1/dec        St0
/bloomfilter1/probe      St1
/bloomfilter1/clk        St1
/bloomfilter1/rst        St0
/bloomfilter1/bout       St0
/bloomfilter1/bin1_high  1110001000000000  1111001011111111
/bloomfilter1/bin1_low   0000110111111110  0000110111111111
```

Fig 7: The output for a mismatch in the Testing

CONCLUSION AND FUTURE WORK

The result above is for the mismatch, in the case when there is an input, which is not the member of the bloom filters database. The AND gate is the most vital parts of the bloom filter block. Its only because of this gate that we can determine the legitimacy of the entry. In certain cases due to the over filling of bits in the hash array table, Its likely to show some level of false positive and false negatives, which are in other terms caused due to mis-mapping.

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