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CNFET-BASED VLSI LOGICAL EFFORT FRAMEWORK

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Abstract: *Carbon nanotube discipline-impact transistors (CNFETs) display fantastic ability to build digital systems on advanced generation nodes with big blessings in phrases of electricity, performance, and area (PPA). But, CNFET-precise extra capabilities together with a variety of tubes, pitch, tube position, and diameter in array of tubes play the massive position in correct PPA evaluation. Furthermore, remember and density versions in carbon nanotube (CNTs) due to manufacturing boundaries, just like a presence of steel tubes inside a CNFET channel, degrade a predicted PPA advantages. Furthermore, modeling a CNFET parameters, CNT versions and etching strategies for CNTs create additional complexity during overall performance optimization. As the result, for realistic optimization of CNFET circuit's performance, it's far vital to comprise an effect of those parameters and versions. In this paper, we suggest put off models for immediate and accurate performance evaluation by using consisting of an effect because of CNFET-precise parameters and CNT versions. For better optimization latest a circuits, we additionally consist of animpact modern day twine parasitic in estimating a postpone today's a man or woman gates. Our optimization device results in a maximum and common postpone development by using 27% and 17%, respectively, and the couple of.5× discount in location for trendy ISCAS and Open SPARC benchmark circuits. Rapid and pretty accurate delay computation in our optimization framework offers notable runtime blessings compared to 497db simulation and statistical-based totally techniques.*

Keywords: *Carbon nanotube (CNT), CNT field effect transistor (CNFET), delay, logical effort (LE), and optimization.*

I. INTRODUCTION

SILICON MOSFET Circuits have skilled tremendous improvements in terms of both overall performance and integration density over a last few decades. However, now, traditional silicon-CMOS gadgets are approaching their physical and technological limits due to version in system parameters and different brief-channel results. Also, transistor scaling faces significant challenges, especially with continuously increasing energy/power dissipation.

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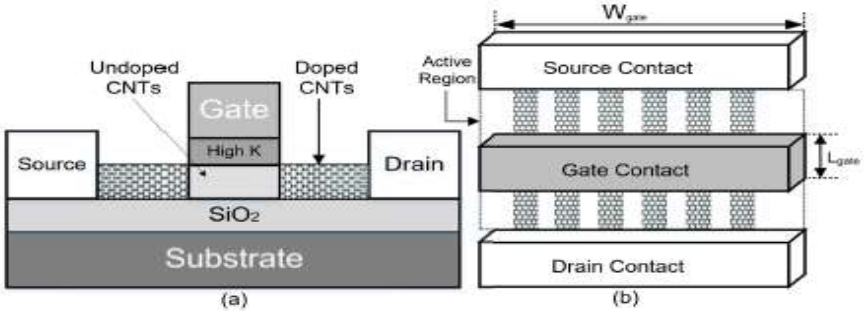

Fig. 1. (a) Side view of the CNFET layout. (b) Top view of CNFET layout with array of six CNTs.

Carbon-based materials such as carbon Nanotube (CNTs) have drawn considerable attention because of advanced electric, thermal, and mechanical properties. CNT field-effect transistor (CNFET) mischaracterized by using extremely-long mean-unfastened course for elastic scattering similar for electrons and holes, high Fermi pace, easy integration of excessive-ok dielectric fabric, and different excellent device characteristics. Furthermore, because of similarities between CNFET and silicon CMOS, a fabrication manner and design techniques from CMOS can be leveraged for CNFET-based circuits. For this reason, CNFET has been taken into consideration as one of recent Promising gadgets for post silicon technology because of their higher current pressure functionality, ballistic shipping, lesser power delay product, and higher thermal balance [5].

It is located thru Deng and Wong that electrical residences of CNFET are no longer precisely a same as of CMOS because of unique CNFET device parameters and traits of CNFET on a top of conventional CMOS-particular parameters such as node voltage, threshold voltage, and gate width, which impact I -V traits of the transistor. A performance of CNFET is impacted with a aid of spacing amongst CNTs due to effect known as screening due to price between two parallel tubes acts as accomplishing channel in parallel. Fig. 1(a) and (b) indicates the go phase and the pinnacle view of the CNFET where an array of six single-wall CNTs are used as the channel material. A fabrication of CNFET-based totally circuits has the few major challenges. The CNT can be each metallic or semiconducting depending on hilarity vector [6]. Nowadays CNT-grown methods produce massive percentage of metal CNTs (m-CNTs) which reason shorts among deliver and drain in CNFET. A ones m-CNTs have to be removed for proper characteristic of CNFET. There are primary strategies to get rid of unwanted m-CNTs: 1) Selective chemical etching (SCE) [8] and the couple of) VLSI properly ideal m-CNT removal (VMR) [9]. Both tube removal techniques get rid of steel tubes near ninety nine. Nine%, but unfortunately, SCE also gets rid of some of desired semiconducting tubes inadvertently, which motives a CNT be counted range and density versions. Any other major challenge is to increase CNTs perfectly aligned and uniformly distributed semiconducting CNTs (s-CNTs). Patil et al. [10] addressed misalignment of CNTs. CNT density version continues to be the assignment and results in lacking CNTs in CNFETs channel. An overall performance, strength, and yield of circuits designed with transistors with CNTs as channel cloth are negatively prompted by way of using these imperfections.

In spite of those challenges, there is substantial research performed to allow consciousness of a CNFET-primarily based digital machine which includes a primary fundamental computer chip a use of CNFET technology by way of Stanford

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Engineers [11]. As the result, it is vital to build excessive-overall performance and strength-efficient circuits primarily based on CNFETs and there's the splendid want to expand validated models for overall performance assessment of CNFET-based circuits. a timing and energy evaluation of CNFET-based circuits is carried out a use of a SPICE model advanced by using Stanford [6], that is used to carry out modern-day-based totally performance analysis and optimizations [12], [13]. For large circuits, dynamic simulations a use of SPICE appear to be the bottleneck. A usage of statistical strategies, like Monte Carlo, for put off analysis in SPICE, inside a presence of CNFET parameter variations, can in addition exacerbate a computation time. For brief and correct performance analysis and circuit-level optimization, there may be crucial need to increase complete framework for CNFET circuits. Lately, some strategies have been suggested inside a technical literature to broaden models to assess performance and yield of CNFET. Cho et al. [14] pointed out a MATLAB based version to analyze a performance of CNFETs for variable CNT spacing at gate stage handiest without presenting any closed-form model for circuit degree. A simulation-based totally linear programming method is provided in [15] on a circuit degree; it's far determined that nonlinear simulations for larger circuits are very time eating, and equivalence dating approach proposed on this paper to calculate parameters imposes difficult requirements to decide parameters required for simulation, which adds up to complexity, mistakes, and runtime. A proposed approach changed into not tested for bigger and complex circuits.

In this paper, we increase complete optimization tool for vicinity and delay minimization in CNFET-primarily based circuits. This device consists of our evolved models based at a enterprise well known logical attempt (LE) framework; pitch-aware LE (light) version, to account for impact of CNFET parameters and role-aware pitch issue (PAPF), to version a CNT count and density versions. a pale and PAPF fashions deal with a venture of lengthy runtime in simulation-based totally techniques for fast and accurate evaluation of energy, overall performance, and vicinity (PPA) of CNFET-based totally circuits. For more practical optimization of a circuit’s performance in pre layout level, we incorporate an impact of cord parasitic at a gate delays. Our novel optimization framework performs circuit-stage techniques (CLTs) to gain optimized fan-out (FO), variety of stages, and branching attempt within a circuit. Those techniques are carried out previous to an optimization of a wide variety of tubes in person gates. A LE method changed into first proposed with a aid of Sutherland et al. And it is utilized in several industry general pc-aided layout equipment and other applications because of its stylish and easy nature. due to competitive time-to-market requirements for most cutting-edge digital CMOS designs, enterprise is focusing increasingly more on shift left strategies, because of this there may be the tremendous hobby for designers to estimate delays of common sense gates and information paths, even throughout a primitive design segment, and to size a good judgment gates so as to meet a timing necessities for higher convergence and timely signoff. A sizing of good judgment gates in order to meet the delay constraints, with minimum electricity dissipation, has been the key requirement in maximum digital designs. Therefore, there has been amazing interested by LE model and full-size research has been accomplished to enhance LE model for MOSFET applications. A standard LE-based totally methodology to estimate yield in presence of versions due to metallic tubes, without incorporating outcomes because of CNFET-specific parameters. An important thing contributions of this paper are as follows.

1) Enhanced LE-based models, PALE and PAPF, for fast and fairly accurate evaluation of an impact of CNFET parameters and CNT variations on circuit delay, which runs 5×–20× as compared to a state-of-the-art algorithms.

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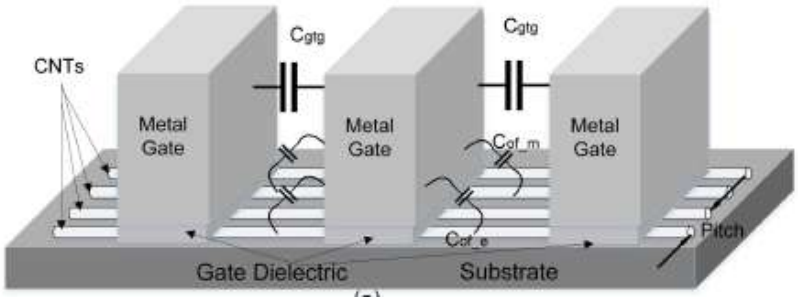
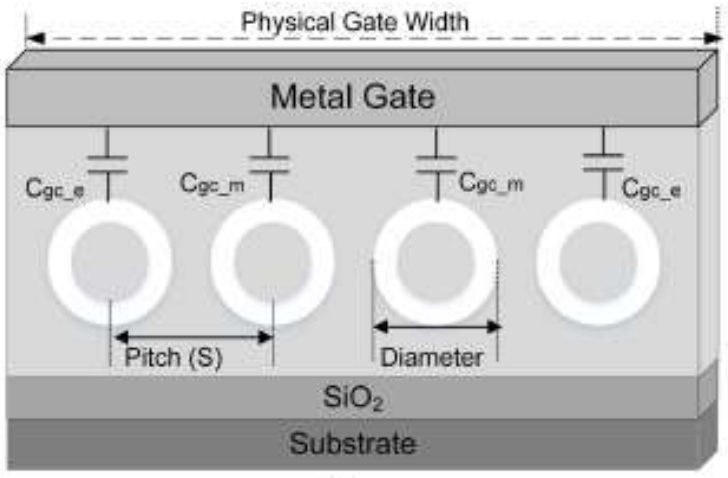
2) Improvement of early format optimization frame work to estimate only quantity of CNTs in a channel to limit place and postpone through considering an impact of CNFET parameters and variations at a gate stage.

3) Incorporating a CLT and wire load in a device to improve a vicinity and put off product (ADP) which helps to satisfy a favored performance at a circuit level. The CNFET-precise parameters, CNFET gate capacitance model, fee screening impact, preferred LE model, and its obstacle for CNFET circuits. Describes a development of LE fashions for CNFET era with rate screening effect thinking about all semiconducting tubes, with CNT density and metallic tube variations. a test outcomes are offered to percentage correlation records of a newly evolved fashions with simulation methods. Discusses a improvement of optimization framework to limit ADP for CNFET-primarily based circuits, by using optimizing the



(a)



(b)

Fig. 2. (a) Three-dimensional structure of a devices with multiple channels and high-k gate dielectric material, and a related parasitic gate capacitances.(b) Cross section of a channel region and a related gate-to-channel capacitances. Number of tubes and performing CLT.

Finally, Section V concludes this paper.

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II. PRELIMINARIES

A. CNFET Gate Capacitance Model

The CNFET 3-D structure is shown in Fig. 2(a). Capacitance fashions for CNFET are taken from [3]. Capacitances related to CNFET are shown in Fig. 2.The exclusive components of C enter gate are proven in (1) and discussed as follows:

$$C_{\text{input\_gate}} = C_{\text{gtg}} + C_{\text{gc}} + C_{\text{of}} \qquad (1)$$

In which Cgtg is a gate-to-gate or gate-to-source/drain coupling capacitance, Cgc is a gate-to-channel capacitance, and Cof is an outer fringe capacitance. Cgtg is a predominant factor of gate capacitance and iscalculated using a system in [3]. it's miles separated into two components, a primary aspect of Cgtg is because of ordinary electric field among two parallel plates and a second one aspect represents fringe capacitance between cylinders. As proven in Fig. 2(a), this capacitance is between steel gates and any effect due to CNTs may be very negligible on Cgtg. Cgc is likewise referred as intrinsic gate capacitance and specific components are shown in Fig. 2(b). There are two sorts of Cgc; Cgc_e is a capacitance of a CNT located inside a fringe of a CNFET device and Cgc_m is a capacitance of a CNT placed in a center of a CNFET tool. a gate capacitance of multichannel CNFETs is calculated by considering a coupling capacitance between a gate and one remoted CNT (Cgc_inf) and an equal capacitance (Cgc_sr) due to rate screening from an adjacent tubes as given in. a price screening is mentioned in element. For 32-nm source/drain period and sixty four-nm gate peak, a contribution of Cof is nearly negligible in comparison to Cgtg and Cgc and which can be not noted.

B. Charge Screening Effect

In an array of CNTs which creates the channel for the CNFET, electric powered discipline traces may be screened due to a proximity of tubes and that might have an effect on a distribution of expenses a various nanotubes[11].This impact is referred to as a screening impact.it is defined by means of Deng et al. [3] with assist of a subsequent equation:

$$C_{\text{inf},01} = \frac{1}{\frac{1}{C_{\text{inf}}} + \eta_1 \cdot \frac{1}{C_{\text{sr},1}} + \eta_2 \cdot \frac{1}{C_{\text{sr},2}}} \qquad (2)$$

where 1 and the couple of are described because a ratio of Cinf,02 and Cinf,03,respectively, over Cinf,01, these are functions of a geometry, a variety of a items of a array, and a placement of an object within a array. Cinf is a capacitance among an electrode or gate and center tube #1 without considering fee screening of all neighboring tubes. Csr,1 and Csr,2 are equal capacitances due to a screening effects of aspect tubes #2 and #3, respectively. Fig. 3(a) indicates N equal tubes in parallel in an array. Fig. 3(b) suggests the simple representationto give an explanation for screening effect and corresponding coupling capacitances. A price distribution due to screening impact affects intrinsic capacitance of the CNFET. At smaller

pitch, a screening effect becomes sizeable and a gate capacitance is not anymore immediately proportional to a wide variety of a CNTs in a channel. essentially, a fee screening reduces a powerful width of a channel, impacts gate-to channel electrostatic capacitance, thereby degrading a tool modern. It means a spacing between an adjoining parallel tubes in the CNFET channel array impacts a pressure electricity of parallel tube transistors because of a screening of rate from adjoining tubes [11]. it is acknowledged that tubes present on a edges of an array have screening from most effective one facet, and tubes in a center get fee screening from adjacent CNTs on both aspects as proven in Fig. three(b). it's far observed that a capacitance of part tubes is two times that of a middle tubes at smaller inter-CNT pitch as shown in Fig. four. This shows that a screening effect is dominant while tubes are separated through small distance which degrades both gate capacitance and current

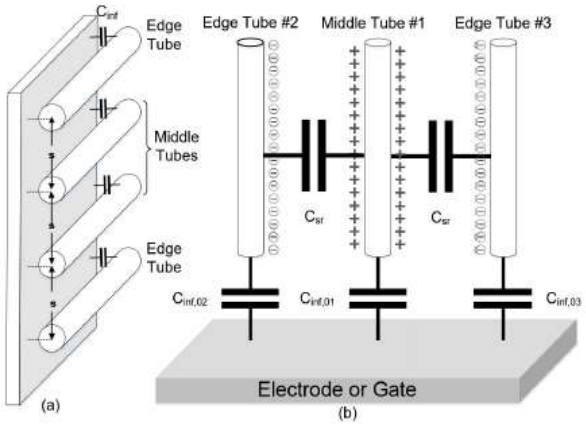

Fig. 3. There are identical CNTs in parallel in an array.

The coupling capacitance Cinf,01 is calculated, through thinking about a outcomes of a CNTs round middle tube #1, which may be lumped into a two nearest CNTs 2 and three on both edges. Cinf,02 and Cinf,03 are equivalent capacitances assuming all other neighboring CNTs are lumped at a location of two and three.

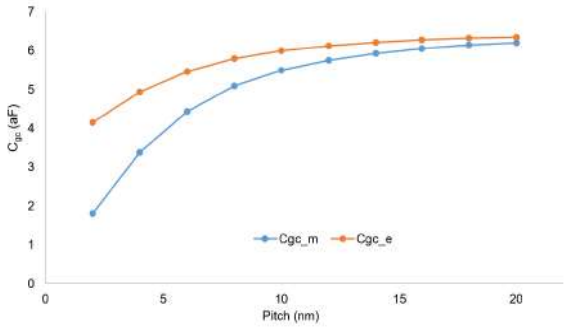

Fig. 4. Impact of charge screening on gate-to-channel capacitance for middle

(Cgc_m) and edge (Cgc_e) CNTs.

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in CNFETs. To avoid overestimating a circuit performance for excessive-velocity CNFET circuits, a screening impact wishes to be taken under consideration [3]. consequently, we've accounted for screening impact in our proposed fashions and discussed in detail.

C. Standard Logical Effort Model

In this section, a standard LE models for CMOS is discussed. a propagation delay of the gates are represented as

$$t_p = (g \cdot h + p) \cdot \tau_0 \qquad (3)$$

$$t_p = d \cdot \tau_0 \qquad (4)$$

wherein zero is intrinsic put off of the reference inverter without parasitic. tp is a propagation put off (also referred as absolute delay) and d is a normalized put off of the gate and is given as

$$d_{\text{norm}} = (g \cdot h + p) \qquad (5)$$

wherein g is a LE of a gate, h is a electrical effort, Cout/Cin, and p is a parasitic (or self-loading) delay. A parameter g represents a enter capacitance required for a no of tubes pitch(nm)

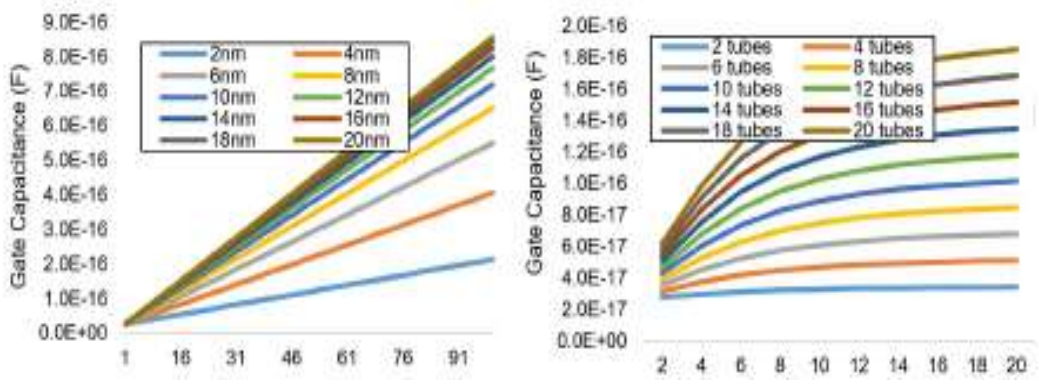

Fig. 5. Gate-to-channel capacitance (*C*gc) for an inverter. (a) Number of tubes in a transistors. (b) Pitch.

gate to have equivalent drive strength as an inverter. LE technique in general calculates the gate delay in termsof a basic inverter delay and input loading of a gate represented as the multiple of a minimum-size transistor's gate capacitance. We use a capacitance-based LE model, whichis defined as a ratio of its input capacitance to that of aninverter that delivers equal output current.

D. Limitations of Standard Logical Effort Model for CNFET

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LE represents a riding functionality of the gate and depend son a gate topology for CMOS devices. It fashions amount of current generated with a aid of the gate whilst the positive price is providedat a enter with steady width. Nowadays generated by the CMOS inverter might be constant for the positive enter voltage applied on a gate of a inverter. however, for CNFET gates, using electricity of the CNFET relies upon at a range of tubes in a channel and spacing between them, which we referredas pitch. therefore, the CNFET gate with steady width outputs different currents for equal enter voltage. LE framework fashions a driving strength of a gates based on a diverse capacitances related to a gate as shown in (1). consequently, we use a CNFET capacitance model to look at a conduct of CNFET enter capacitance in a presence of charge screening. We examine impact of a number of CNTs and pitch at a input gate capacitance of CNFET. In Fig. 5(a), we show a conduct of gate capacitance with a variety of tubes within a gate. it is able to be seen that a gate capacitance of CNFET gates varies linearly with a number of tubes. however, Fig. 5(b) suggests that at smaller pitch values, e.g., 6 nm and below, effect of fee screening on Cgc is extra visible. It varies with CNTs spacing and has nonlinear effect at a gate input capacitance. A slopes of Cgc advise that a riding capability of CNFET varies differently with wide variety of CNTs for numerous pitch values. therefore, it is important to model impact of screening effect on input gate capacitance for correct put off assessment ofCNFET-based totally circuits.

III. PROPOSED MODELS FOR CNFET LOGICALEFFORT FRAMEWORK

In this segment, improvement of a proposed models for CNFET generation for best cases (considering screening effect without the CNT versions) and realistic cases(with CNT density and metal tube versions). We also present correlation of evolved fashions a use of simulations methods.

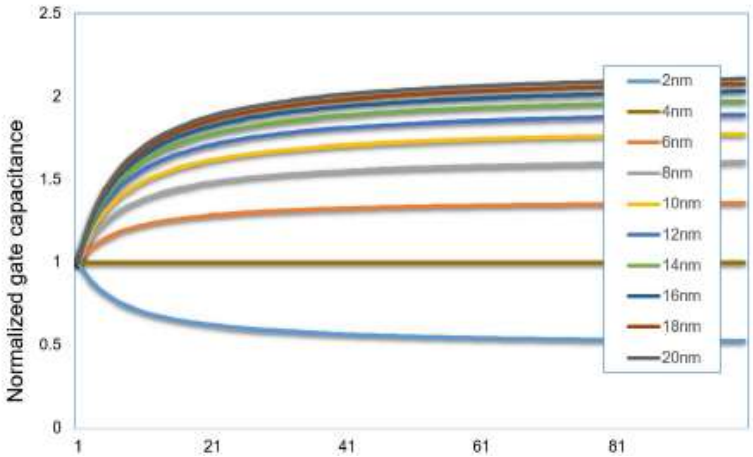

Fig. 6. Input capacitance of an inverter with given pitch normalized withrespect to reference inverter CNT pitch (4 nm).

A. Pitch-Aware Logical Effort Model

As the way to increase a LE version for CNFET gates, we use 32-nm generation node for our model improvement. As discussed in [14], LE version evaluates postpone of common sense gates normalized to the reference inverter. A reference

inverter in CNFET has a minimal gate width of 32 nm. As we just discussed in phase II-E that there can be multiple combinations of range of CNTs and pitch for identical width of a inverter. We decide to select our reference inverter for CNFETs based totally at a favored CNT density (250/μm) to in shape overall performance of CMOS circuits [6]. A favored density calls for at least eight CNTs for a minimal width inverter. as the result, our reference inverter has 8 tubes separated through 4-nm spacing. A delay of inverters and other logic gates with one-of-a-kind quantity of tubes and pitch mixtures is normalized with respect to a reference inverter. to evaluate a CNFET velocity, it is proven in [3] that a pressure present day is proportional to a gate-to-channel capacitance in step with unit channel length Cgc, and nearby interconnect series resistance is normally plenty smaller than a CNFET universal intrinsic resistance; consequently, CNFET postpone is proportional to a input gate capacitance and represented as

$$t_p \propto \frac{C_{gc} \cdot L_g + 3(C_{of} + C_{gtg} \cdot W_{pitch})}{C_{gc}} \qquad (6)$$

Wherein Lg is a physical gate duration, and Wpitch is a device pitch in a width direction, both of these phrases are steady. In (3), tp is represented inside a form of LE version expression and is proportional to normalized postpone of a gate and delay of a reference inverter without parasitic. consequently, to model a screening effect for LE framework, Cgc of inverter with positive CNT spacing is normalized with recognize to reference inverter CNT pitch (4 nm). An outputs from multiple simulations are summarized in Fig. 6 for distinctive Ntur and pitch values. it may be seen that effect of screening on normalized gate capacitance is the lot large at smaller CNT spacing. also, a normalized gate capacitance varies from zero.five to two.2× of a reference inverter. We pick out a cost of normalized gate capacitance, referred as the pitch element (PF) for every pitch cost where

TABLE I LUT:

PF VALUES FOR DIFFERENT SPACING BETWEEN CNTS

Pitch (*nm*)	2	4	6	8	10	12	14	16	18	20
PF	0.5	1.0	1.3	1.4	1.5	1.57	1.62	1.67	1.7	1.73

the curve for inverter gate capacitance reaches saturation. within a first-order approximation, PF captures a nonuniform behavior of normalized Cgc inside a presence of fee screening for extensive range of pitch values such as due to each area and middle CNTs inside a CNFET channel, which is wanted in simple expression shape for a LE framework., that's referred as lookup table (LUT), shows a values of PF for huge range of CNT pitch. Be aware that a reference pitch of four nm has a PF of one. considering that, a screening impact has an inverse impact at a riding capability of a gate, subsequently, nonlinear effect of screening is modeled as 1/PF in (7). also, inverse linear impact of CNT expect LE (g) as proven in Fig. 5(a) may be captured because a ratio of tubes in the certain gate to a reference inverter (Ntur/Nref). As the result, this PF and ratio of tubes are included inside a LE framework to model a driving strength of a inverter at unique CNT spacing and counts. therefore, a newly evolved LE model is referred as faded and proven within a following equation:

$$g' = g \cdot \left(\frac{1}{\mathrm{PF}}\right) \cdot \left(\frac{N_{\mathrm{ref}}}{N_{\mathrm{tur}}}\right). \quad (7)$$

The normalize delays in a presence of screening effect is presented as

$$d^r = g^r \cdot h + p. \quad (8)$$

Equation (4) for CNFET-based circuits is represented as follows:

$$t_{p,\mathrm{CNFET}} = d' \cdot \tau_0 = \left(g \cdot \left(\frac{1}{\mathrm{PF}}\right) \cdot \left(\frac{N_{\mathrm{ref}}}{N_{\mathrm{tur}}}\right) \cdot h + p\right) \cdot \tau_0. \quad (9)$$

it's far found that large Ntur and pitch values lead to decrease attempt required by means of a gate to drive a load. Because a CNT spacing will increase, impact of screening impact reduces and a fee of PF increases. An increase in PF reduces g showing a better driving power of a inverter, for this reason progressed put off, i.e., tp $\propto$ (1/PF). to house PF inside a common LE framework in a form of expression, it could be represented as proven in a following equation rather than LUT:

$$\mathrm{PF} = \frac{(2 \cdot P_{\mathrm{abs}} - 2)}{(P_{\mathrm{abs}} + 2)} \quad (10)$$

wherein Pabs represents absolute value of CNT pitch and normalized to (CNT pitch(nm)/1 nm). for this reason, (9) is up to date as follows to calculate a propagation postpone of any good judgment gate:

$$t_{p,\mathrm{CNFET}} = \left(g \cdot \left(\frac{(P_{\mathrm{abs}}+2)}{(2 \cdot P_{\mathrm{abs}}-2)}\right) \cdot \left(\frac{N_{\mathrm{ref}}}{N_{\mathrm{tur}}}\right) \cdot h + p\right) \cdot \tau_0. \quad (11)$$

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TABLE II

COMPARISON OF DELAY FROM LE MODEL AND SIMULATIONS FOR THREE-STAGE DECODER, WITH B = 8 AND H = 9.2

Gate Width	CNT Pitch	No. of Tubes per Transistor	Logical Effort (g)	Normalized Delay (d_{norm})	Absolute Delay (d_{abs}) (ps)	Model runtime(sec)	Simulations (d_{sim})(ps)	Simulations runtime(sec)	Δ Delay(%)
32nm	2nm	16	5	27.49	12.92	0.117	13.377	270.27	3.38
	4nm	8	2.5	23.06	10.83	0.117	10.956	333.52	1.06
	8nm	4	3.57	25.21	11.85	0.117	12.192	352.3	2.78
	16nm	2	6	28.84	13.55	0.117	13.438	336.01	0.88
45nm	3nm	15	2.08	22.05	10.36	0.117	10.417	279.81	0.48
	5nm	9	1.70	21.00	9.87	0.117	9.823	303.17	0.51
	9nm	5	1.89	21.54	10.12	0.117	10.165	318.92	0.37
	15nm	3	2.45	22.96	10.79	0.117	10.417	291.7	3.61
60nm	2nm	30	2.66	23.43	11.21	0.117	12.003	281.01	6.57
	3nm	20	1.56	20.58	9.67	0.117	9.769	315.72	0.94
	4nm	15	1.33	19.83	9.32	0.117	9.169	313.77	1.68
	5nm	12	1.27	19.63	9.22	0.117	9.026	312.98	2.24
	6nm	10	1.28	19.65	9.23	0.117	9.097	320.83	1.52
	10nm	6	1.48	20.33	9.55	0.117	10.14	310.94	5.82
	12nm	5	2.59	23.26	10.93	0.117	10.79	309.73	1.31
	15nm	4	3.6	25.26	9.87	0.117	9.767	298.69	0.92
	20nm	3	5.95	28.79	13.53	0.117	13.365	314.86	1.25
	30nm	2	5.51	28.21	13.26	0.117	13.731	327.62	3.42

The active place of the CNFET causes supply–drain to short and referred as quick disorder (CNFET1). The CNFET may be the "purposeful" if it encounters neither open nor short defects (CNFET2 and CNFET3). Fig. 7(b) shows a type of the CNFET based at above-referred to description. If a capability of the CNFET changes because of either an open or the brief defect, it is considered as defective. As mentioned formerly that a two methods, SCE and VMR, are used to put off unwanted metal tubes. the given percentage of metal tubes is diagnosed by means of Pm issue and overall percentage of tube removed is given with a aid of Pr. a SCE eliminates a steel tubes but may gets rid of the number of a semiconducting tubes. A percentage of semiconducting tubes eliminated depends on a diameter of a tubes. A VMR is the notably efficient technique, getting rid of all a metal tubes best. each of those metallic tubes removal techniques motive CNTs density versions within a CNFET channel, which ends up in nonuniform pitch as shown in Fig. 7(c). To account for nonuniform pitch effect, a analytical version for a gate-tochannel capacitance (Cgc) may be rewritten for tubes inside a center [38] and is given by using (12), shown at a lowest of a subsequent web page, which incorporates impact of nonuniform pitch among tubes on a rate screening impact since a pitch on either facet of the center tube may be unique if adjoining tube is eliminated, where P1 and P2 are a pitches on a both aspect of a center tube. As shown in Fig. 7(c), P1 and P2 values for the tube will depend on a fee screening of tubes on both aspect. A neighboring metallic tubes and their elimination may also boom either or each P1 and P2. however, a brink tube has handiest one pitch value which depends on screening effect of adjacent tube as given through

$$C_{gc\_e} = \frac{1}{C_{gc\_inf}} + \frac{1}{C_{gc\_m}}. \qquad (13)$$

Moreover, Monte Carlo simulations are used to generate a sample population of common sense gates, using sample tubes with diameter levels from 1 to 2 nm, that is required to assemble a given variety of gates for statistical analysis. a random elimination of tubes using SCE and VMR results in nonuniform pitch distribution in transistors. In our evaluation,

we've got assumed that a proportion of metal tubes present is among 0% and 25%. We use 1.four nm as diameter threshold for a elimination of semiconducting tubes as advised in [8] for SCE. We also assume that no transistor has much less than two tubes after a removal system. A gate-to-channel capacitance for each tube is predicted primarily based on its position and neighboring tubes using (12). An influence of nonuniform pitch is also considered for a threshold tubes. A capacitance of each tube within a tube array for every transistor array is summed as much as attain a entire capacitance of every gate. An inverter gate capacitance for given number and role of a tubes eliminated is normalized to best case with no metallic tubes. we've got conducted the detailed evaluation to look at impact of a range of tubes eliminated from the sure position on a normalized gate capacitance that is posted in [23] along with a preliminary PAPF implementation. it's miles obtrusive from a experiments that initial assumptions of the uniform pitch after a elimination of metal tubes [22] introduces great error in a delay estimation. An imply capacitance of a given population of inverter gates for one-of-a-kind values of Pm is calculated. A reference inverter with Pm = 0% is used to normalize a suggest capacitance of inverter gates fee at every Pm price.The PAPF in (14) models a conduct of normalized capacitance for given Pm and Pr based on a applied elimination approach. health component α represents a σ/μ at Pm = zero and captures distinctive stages of transistor

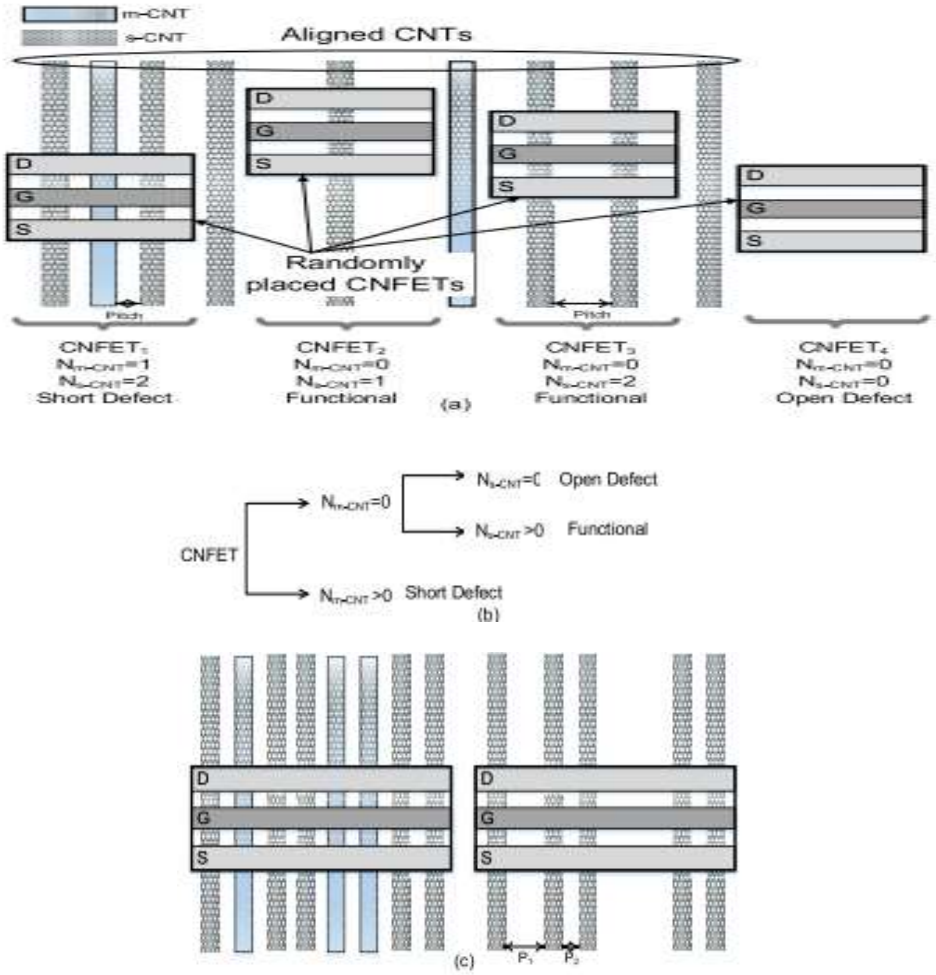

Fig. 7. (a) CNFETs randomly placed on aligned s- and m-CNTs. Nm−CNT represents a number of m-CNT and Ns−CNT expresses a number of s-CNT in the CNFET. CNFET2 and CNFET3 are functional where CNFET1 and CNFET4

have short and open defects, respectively. (b) Classification of CNFETs defects based on a number of m- and s-CNTs placed in an active region. (c) Impact of metallic tube removal resulting in nonuniform pitch.

tubes (N_{tur})

$$\text{PAPF} = (1 - \alpha \cdot (x \cdot P_m + (1 - x) \cdot P_r)) \quad (14)$$

where $\alpha = (\sigma/\mu)_{P_m=0} = 0.005$, $x = 1$ for VMR, and $x = 0$ for SCE. Now, the LE model can be represented as follows:

$$g' = g \cdot \left(\frac{1}{\text{PAPF}}\right). \quad (15)$$

Normalized delay can be calculated by

$$D_{\text{norm}} = g' \cdot h + p. \quad (16)$$

The normalized capacitance values at unique Pm values for CNFET with extraordinary tube array sizes.

IV. OPTIMIZATION OF CNFET CIRCUITS

As mentioned within a creation section, most of a proposed methods and techniques might also help to enhance a performance of a gates or to make certain that a gates are functional. But, impact of vital circuit-stage parameters is overlooked including twine parasitic, variety of ranges, FO, and branching attempt and so on inside a CNFET circuits. Consequently, those strategies have confined answer space which may additionally bring about a neighborhood optima. In this phase, we endorse comprehensive performance and vicinity optimization framework for CNFET circuits primarily based on advanced faded and PAPF LE models and a huge-scale gate sizing (LSGS) set of rules from [39]. a prevailing work [39], [40] modeled a combinational circuits as the geometric programming trouble and offered a technique for instant optimization of CMOS gate sizes. a key features evolved for CNFET-based totally circuits as part of LSGS set of rules are discussed as follows.

1) Implementation of CLT, including optimizing a wide variety of levels, a FO, and branching effort, to reap global optima in addition to optimization of number of CNTs or gate sizing in the CNFET.

2) Incorporating effect of wire parasitic at a circuit performance for greater practical and accurate optimization a use of rent's rule technique to obtain a cord-period distribution of every circuit.

3) Implementation of light and PAPF LE fashions to consist of impact of CNFET screening and CNT density variations in a course of optimization to satisfy a preferred overall performance specifications appropriately.

A. Optimization methodology on this phase, we gift the complete methodology and steps for optimizing a performance and area of CNFET circuits.

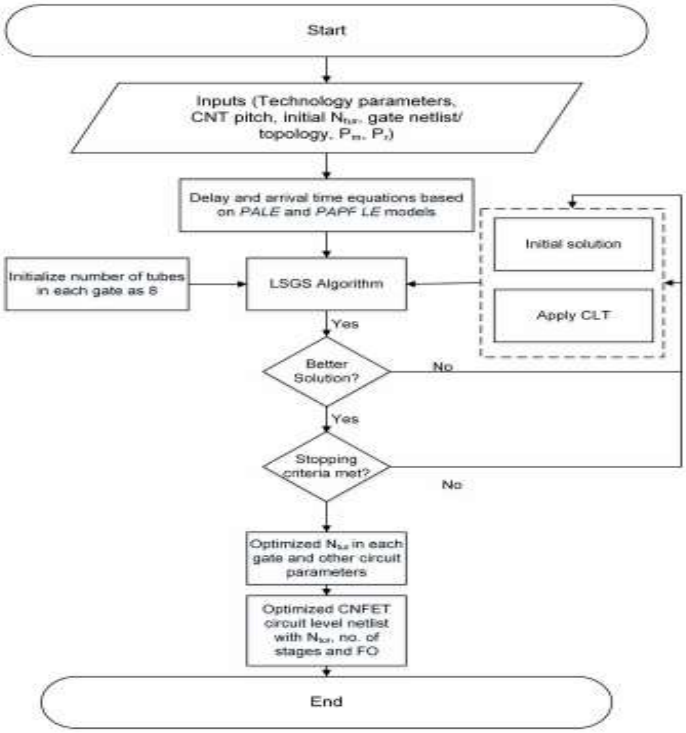

Fig. 8. Flow diagram of optimization framework for CNFET-based circuits.

1) Optimization go with a flow: a waft diagram of evolved optimization framework is proven in Fig. eleven. a technology parameters which include CNT pitch, initial Ntur, percent of steel tube (Pm), percent of removed tubes (Pr), etching strategies such as VMR or SCE, gate netlist, and circuit topology are supplied as input to a optimization framework. We write equations for delay and arrival time for each gate based totally on light and PAPF-based LE fashions for ideal and sensible instances with steel tubes and density variations, respectively.

2) cost function: a goal function of a hassle is a optimization of gate sizes to acquire a minimal region assembly a favored timing specifications, as shown inside a following equation:

$$\min_{(\text{area})\in\mathbb{R}} C(x) = \text{area}$$
$$\text{s.t.} \sum_{i=0}^{n} d_i^{\text{path}} \le d_{\max} \qquad (17)$$

where dpath i represent a delay of a ith gate in the certain path and dmax is a upper bound on a gate delays. a LE frame worked suggests that a number of stages can be critical in determining overall delay of a circuits.

In our algorithm, it is executed by using randomly deciding on a nets and including/disposing of even number of buffers from a circuit without changing a capability. FO of a crucial nets is optimized before doing a sizing of all a gates. It allows starting an optimization section with the better synthesized net listing, useful for an algorithm to converge with worldwide greatest answer. A price feature is evaluated at each generation till preventing standards are met. Our set of rules terminates if the sure range of iterations defined by means of a person are reached or desired timing specs are met. A

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effectiveness of our method in enhancing a location and performance of a benchmark circuits is discussed within a outcomes segment. A optimization set of rules is shown in advance and steps are discussed as follows.

1) Initialization: inside a first step, all a gates are assigned initial number of tubes to decrease put off, represented as the vector x. a minimum postpone of every gate is computed a use of pale and represented as dmin vector. a cord load for every gate is computed a use of lease's rule and represented as okay vector. A primary outputs are assigned a most load fee. A gate connectivity is represented as FO matrix, which defines fan-out for each gate. An initial place and postpone of each gate are computed based totally on x, dmin, ok, and FO.

2) Timing Specification: We defined a timings specification vectors (T) that each circuits is require to meet. A length of a vectors T defines a numbers of iterations.

3) Apply CLT: We applying certain CLT to optimize a performances of a circuit prior to tubes optimization. These techniques are categorized as:

1) optimize a numbers of stage (buffer insertion);

2) optimizing branches effort;

3) FO optimization; and

4) optimizing gating sizes. This technique is applied to individual net of each iteration prior to tube optimization.

Tube Optimization: After appearing CLT, we optimize a wide variety of tubes in every gate to reduce a full location such that a maximum put off of each route does not exceed a timing specified in step 2). This step is completed using a LSGS set of rules. five) preventing standards: a set of rules terminates after the positive wide variety of iterations. A range of iterations is described by means of timing specification. A very last output of a go with a flow is an optimized gate sizes, put off of each gate, and place of a circuit. B. Parameters Estimation in this segment, we describe a strategies used for estimation of parameters defined inside a fee feature.

1) Delay Estimation: a postpone of every gate is represented in (18) and depends on its length and size of load it drives

$$D_i = d_i^{\min} + \frac{g_i + \sum_{j \in FO(i)} F_{ij} x_j}{x_i}, \quad \text{where } i = 1, 2, \ldots, n. \tag{18}$$

Instead, a delay models in (18) can be represente as RC delay models of gate or wire as shown in (19). Here, ri , cint i , or cin i are a driving resistance, internal capacitance,

Algorithm 1 Optimization Algorithm

```
x=initial number of tubes (gate size);
d_min=minimum delay of each gate;
k = wire load of each gate;
FO= fan-out;
area= initial area;
delay = initial delay based on d_min, k and FO;
T=timing specification vector;
while itr ≤ length(T) do

    Apply CLT
    a_min = minimize area s.t. d_max ≤ T
    new_x = x + (apply CLT+a_min)
    new_area = area + (apply CLT+a_min)
    new_delay = delay + (apply CLT+a_min)
end
return (new_x, new_area, new_delay)
```

and a input capacitance of the minimal-size inverter of gate i, respectively. ci is a wire load capacitance for gate i. it's far assumed that inner capacitance and enter capacitance of gate scales linearly with a dimensions component, and consequently, it is represented as cjin

$$D_i = r_i x_i \left(c_i^{\text{int}} x_i + c_i^{\text{wire}} + \sum_{j \in \text{FO}(i)} c_j^{\text{in}} x_j \right). \qquad (19)$$

The similarity among timing model in (18) & (19) can be represente as follows:

$$d_i^{\min} = r_i c_i^{\text{int}}, \quad g_i = r_i c_i^{\text{wire}}, \quad i = 1, 2, \ldots, n,$$
$$F_{ij} = \begin{cases} r_i c_j^{in}, & j \in \text{FO}(i) \\ 0, & \text{otherwise.} \end{cases}$$

however, in our implementation, dmin i for CNFET gates is expected primarily based on faded. If there are not any metal tubes inside a circuit, (Pm = 0%), inner delay of a gates is obtained a usage of PF from (7) and (10), which relies upon on CNTs pitch and their count number. however, for Pm more than 0%, a put off of a gates additionally depend upon a position of steel tubes removed, and it is anticipated using PAPF LE model from (14) and (15)

$$d_i^{\min} = \begin{cases} \dfrac{r_i c_i^{\text{int}}}{\text{PF}}, & P_m = 0\% \\ \dfrac{r_i c_i^{\text{int}}}{\text{PAPF}}, & \text{otherwise.} \end{cases}$$

2) Impact of twine Load and Estimation: a twine load for output gates is computed primarily based at a twine-duration distribution obtained for every benchmark circuit using rent's rule. we've used a longest cord to compute a cost of constant load pushed by all of a output gates. An inclusion of twine parasitic is essential for practical optimization of tubes and gate sizes for CNFET circuits. We take an example of small ISCAS benchmark circuit (c17) to expose that a impact of wire load. a gates #five and #6 are a output gates and force regular twine load defined by using a minimum, common, and most

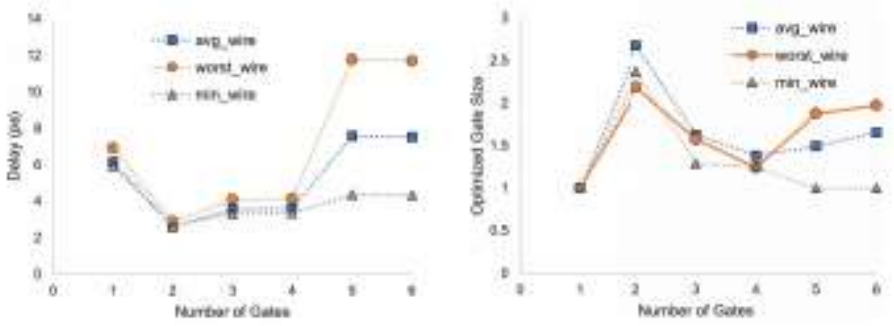

Fig. 9. Impact of wires on a (a) delay of c17 circuit and (b) optimal gate sizes of c17.

(worst) wire length. Fig. 9(a) suggests that a delay of output gates range extensively below one of the kind twine load and cannot be omitted for a duration of a optimization. If we ignore a effect of wires in a course of optimization, we may additionally get surest gate sizes for minimum wire as proven in Fig. 9(b). however, a top of a line gate sizes needed for worst length are double of a minimal cord. for this reason, our optimization algorithm takes impact of cord load into consideration and optimize a gate sizes higher for normal minimization of a location and delay. similarly, cwire i in our algorithm is computed using hire's rule [4] given with a aid of (20). A longest twine acquired from a wire-duration distribution is used to calculate a entire cord capacitance. A capacitance in keeping with unit duration for 32 μm (zero.2 fF/μm) is multiplied through a longest wire within a circuit to reap cord capacitance which acts as load for all output gates. A put off estimation and optimization are done, thinking about the consistent wire load, which results in better optimization of circuit overall performance. since a number of buffers and their positions aren't recognized until placement and routing degrees, so we have neglected their impact at a cord put off estimation at some stage in optimization

$$\textit{Region I: } 1 \le \ell \le \sqrt{N}$$
$$i(\ell) = \frac{\alpha k}{2}\Gamma\left(\frac{\ell^3}{3} - 2\sqrt{N}\ell^2 + 2N\ell\right)\ell^{2p-4}$$
$$\textit{Region II: } \sqrt{N} \le \ell \le 2\sqrt{N}$$
$$i(\ell) = \frac{\alpha k}{6}\Gamma\left(2\sqrt{N} - \ell\right)^3\ell^{2p-4} \qquad (20)$$

in which is a length of interconnect in units of gate pitches, N is a wide variety of good judgment gates, p is lease's exponent, α is a fraction of a on-chip terminals appearing as the sink and depends on common FO given by

$$\alpha = \frac{\mathrm{FO}}{\mathrm{FO}+1} \qquad (21)$$

and Γ is given by

$$\Gamma = \frac{2N(1-N^{p-1})}{\left(-N^p\frac{1+2p-2^{2p-1}}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{N}}{2p-1} - \frac{N}{p-1}\right)}. \qquad (22)$$

3) region Estimation: a overall location of CNFET circuits is given inside a following equation, wherein ai is a location of a minimum-length ith gate, and xi represents a optimized size of ith gate at every iteration

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$$\text{area} = \sum_{i=0}^{n} a_i x_i. \qquad (23)$$

Table III

Total Delay And Area Of Iscas And Opensparc Benchmark Circuits With Tube Optimization And With Tube + Clt Both Including Runtime Comparison Of Our Algorithm With Lm And Nlm On the Single 2.6-Ghz Processor With No Parallelization

ISCAS											
Circuit	Area		Total Delay (ns)						Runtime (sec)		
			Ideal case (P=4nm)			Metallic tube variation					
	Actual (μm)	Optimal (μm)	w/o CLT	with CLT	Δ(%)	w/o CLT	with CLT	Δ(%)	Our Algorithm	LM	NLM
c17	86.0	48.224	0.061	0.058	- 4.2	0.063	0.059	-3.1	0.2	201.5	1.63e+4
c1355	2.97e+04	1.49e+04	17.51	13.29	-24.2	17.96	13.72	-23.7	12.2	530.7	5.64e+4
c3540	7.62e+04	3.81e+04	61.77	48.18	-22.1	63.06	49.63	-21.3	57.1	1068.2	1.22e+5
c5315	1.05e+05	5.72e+04	96.98	73.65	-24.1	99.57	75.93	-23.8	156	1504.9	1.75e+5
c7552	1.63e+05	8.20e+04	145.1	116.0	-22.1	149.8	119.2	-20.5	369	2055.2	2.42e+5
10k	2.15e+05	1.08e+05	220.4	178.0	-19.3	226.4	183.2	-22.4	522	2657.4	3.15e+5
OpenSPARC											
des3_area	8.12e+04	2.04e+04	96.54	93.14	-3.6	102.26	97.82	-4.4	185	1.44E+03	1.66E+05
aes_core	3.76e+05	9.40e+04	396.34	374.98	-5.5	409.78	379.3	-7.5	4510	4.99E+03	6.45E+05
wb_conmax	4.83e+05	1.21e+05	1076.12	879.59	-18.3	1152.26	888.89	-22.9	8380	1.15E+04	9.00E+05
ethernet	7.47e+05	2.87e+05	4027.5	2939.9	-27	4135.7	3205.6	-22.5	18300	2.60E+04	1.81E+06

The powerful width of each gate is a made of a assigned variety of tubes to a gate and given CNT spacing. a made from calculated width and given duration (era) of a channel is described as a location occupied through each transistor within a gate. a overall circuit area is acquired by means of a summation of vicinity occupied with a aid of every gate depending on a connectivity of each gate inside a circuit. C. experiment results on this phase, we gift overall performance and a location of CNFET circuits a use of evolved optimization tool. we've used ISCAS-85 and OpenSPARC benchmark circuits for those experiments. An intrinsic delay of each gate is predicted using our pale and PAPF fashions. A cord length for each circuit is computed a usage of lease's rule, and rent's exponents are p = 0.75, ok = three.8, and FO = 2.8. it is assumed that each output gate is riding the constant twine load determined primarily based at a cord-length distribution of a circuit. desk V gives a location and general postpone of ISCAS and OpenSPARC benchmark circuits for ideal case and with metal tubes versions. A delay of gates consists of its intrinsic delay, in addition to a delay because of driving other gates or constant wire load. a introduction of CLT previous to tube optimization improves a delay inside a circuits through as much as 27% for both perfect and sensible eventualities. a boom in general delay because of a presence of 25% metal tubes is around three% on average. This indicates that a general effect of tube elimination on a overall performance of CNFET circuits averages out because of removal of tubes from input and FO gates. Our set of rules also reduces a total place with an aid of more than 2× for all benchmark circuits. a giant discount in total postpone is due to tremendous decline in a worst put off which can be attributed to unoptimized FO or ranges inside an important paths. we've got run experiments using our optimization device with light model for large OpenSPARC benchmark circuits with excessive gate matter, greater complexity, and higher reconvergent

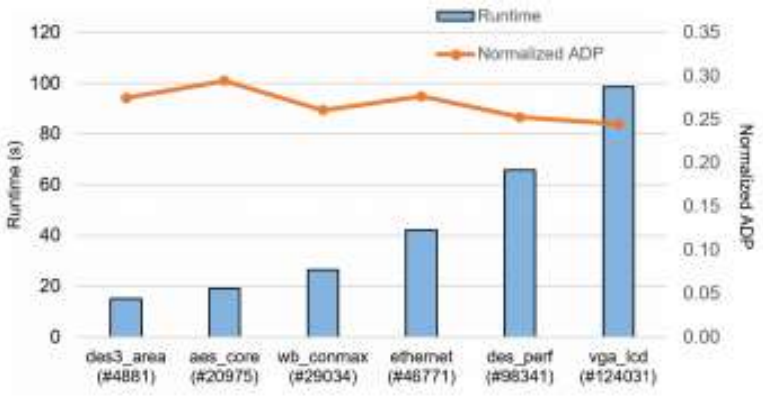

Fig. 10. Runtime and normalized ADP after tube optimization for different sizes of OpenSPARC circuits.

FO to illustrate a scalability of a proposed set of rules as shown in Fig. thirteen. It shows a runtime and normalized ADP with tube optimization for one-of-a-kind sizes of OpenSPARC modules. A normalized ADP is a ratio of ADP with tube optimization to a ADP without any optimization. it is discovered that a common normalized ADP of examined modules is around zero.27. Fig. 14 indicates a delay distribution of person gates in 10-k circuit with and without a CLT. A encircled location suggests a put off of an important gates exceeding 100 playstation and drastically impacting a worst and total postpone in a circuit. it may be determined that our set of rules allows to decrease a delay of those vital gates, which allows in decreasing overall postpone. An effects recommend that earlier circuit optimization enables to obtain international optima, in place of tube optimization which may additionally give simplest nearby optimal solution. it may be concluded that our optimization set of rules allows lowering a delay in essential gates, thereby improving a region and a performance of a circuit. We evaluate a runtime of our set of rules with a runtime of optimization algorithm discussed in [16] a use of a linear model (LM) and nonlinear timing fashions (NLM) for CNFET circuits postpone computation. A mentioned runtime in desk V for NLM and LM for ISCAS and OpenSPARC benchmark circuits is expected primarily based on a pronounced gate count, comparable optimization alternatives, and machine specification, which is cheap assumption for runtime comparison.

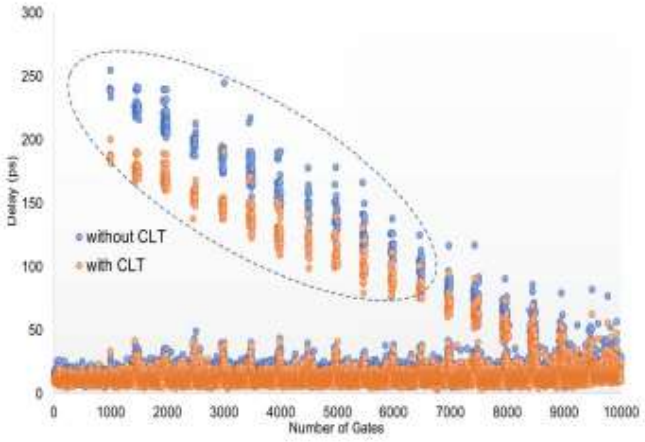

Fig. 11. Delay Distribution of Gates in 10-k circuit.

The Existing of CNFET circuits in optimization framework [16] is predicted a usage of Monte Carlo statistical timing analysis approach as defined in [14]. However, Hills et al. [6] linearized a nonlinear timing version in [14] to analyze a effect of CNT versions on CNFET circuit put off variations. In our optimization algorithm, we use PAPF version for brief and pretty accurate estimation of postpone within a presence of CNT versions. This reduces a general runtime of our set of rules notably as compared to LM and NLM. It have to be cited that objective feature in [6] is to decrease power beneath put off constraints. While, in our fee characteristic, a location of CNFET circuits is minimized to meet precise timing constraint. Our optimization tool suggests the sizeable runtime development over LM and NLM, as proven in table V.

V. CONCLUSION

This paper describe a frame work for delay or minimize of CNFET bases on VLSI circuit in view of a impact of CNFET-specific parameters or CNT variation. It is very critical in of CNT pitch, tubes, CNTs density and metallic tube variations are critical in determining a PPA of CNFET-based VLSI circuits. A parameter and variation may not be ignore a true performance optimization of CNFET.

Applying CLTs prior to tube minimization in CNFET circuit, helping to achieve a global optimum solutions, reducing a delay in a benchmark circuits by up to 27% or area by 2.5×. inclusion of wire parasitic loads is essential for achieve optimal number of tube in a CNFET gate or for a true optimization of area & delay in a circuits. An increment in delays on a presence of 25% metallic tubes are below 5% indicate that overall impacts of tube elimination on a performing of CNFET circuit averages out. An use of fast or mostly accurate LE-base model for an evaluation of delay in CNFET circuit helped in reduce a runtime of optimization algorithms significantly, compared existing simulation or statistical method. a developed LE-bases frameworks can be productively deploy in early design cycle and prelayout stages of a design phase for more realistic evaluation and optimization of a CNFET-base VLSI circuit. Future research focusing include a following.

1) Adding of a power components to optimize a frameworks on conjunction by presentation or area for more complete analysis.

2) Incorporate a parallelism using distribute machine processed approach to further improving runtime of our tool.

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