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Design and Analysis of 8-bit Array, Carry Save Array, Braun, Wallace Tree and Vedic Multipliers

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Abstract--- *Multiplier is the basic building blocks for several applications like digital signal processing processors, digital image processing. In this paper, we have designed 8-bit array, carry save array, Braun, Wallace tree and Vedic multiplier. And we have analyzed speed, area and power. Design was implemented using verilog HDL coading simulated and synthesized using Xilinx Tool.*

Index Terms--- *Array Multiplier, Carry Save Array Multiplier, Wallace Tree Multiplier, Braun Multiplier, Vedic Multiplier.*

I. INTRODUCTION

Multipliers play important and significant role in Signal Processing according to A. V. Oppenheim and R. W.

Schafer [1] and other various applications. Multiplication is mathematical operation in which the number is added to itself for the specified number of times. Multipliers take more time and area than other arithmetic operations. Multipliers are used in Digital Signal Processing applications such as convolution, filtering, Fast Fourier Transform (FFT) and in Arithmetic Logic Unit(ALU) in microprocessors. 8.72 % of all the instructions in scientific program are multiplication as per A. V. Oppenheim and R. W. Schafer [1]. Researchers have been carried by Poras T. Balsara et al. [7] ,R. Gnanasekaran [8], Gensuke Goto, Tomio Sato et al. [9],H. I. Saleh, A. H. Khalil et al. [10] to develop new techniques and algorithms for high speed and optimized area.

An efficient multiplier has the following characteristics Speed: The Multiplier should perform the operations at high speed.

Accuracy: The results of Multiplier should be correct. Area: Multiplier should occupy less area that is it should be with minimum no of transistors.

Power: Power consumption of Multiplier should be low.

Multiplication operation generally comprises of two steps.

Partial Products are generated in the first step and then it is added with the previous partial products. Every bit of multiplicand is multiplied by every multiplier bit to get partial products. So to multiply two N-bit numbers N partial product rows of N bit each has to be generated. So we need AND gate to generate every bit of partial product.

The general process can be broken down into three steps as per H. A. Al-Twaijry [2] as shown in Figure 1.

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1. Partial products are generated in the first step. The partialProducts are generated in parallel and there are several ways for partial products generation.
2. Reduction of Partial Products are reduced from N rows totwo rows which are called as sum and carry rows. Special adder architectures are used to produce the final two rows.
3. The delay of this step can be reduced upto 30 % as per Earl E. Swartzlander, Jr. [5].
4. The two rows sum and carry rows are added using Adderto get the final product of the input operands.

The following multipliers are simulated and synthesized

1. Array multiplier
2. Wallace multiplier
3. Braun multiplier
4. Carry save array Multiplier
5. Vedic multiplier In this paper, we analyze and compare area,speed, power of different multipliers using Verilog HDL. The Figure 3 shows Serial Multiplier. The Figure 4 shows Parallel Multiplier.

Array Multiplier

The Figure 5 shows regular well known structure of Array Multiplier. In this Multiplier the partial products are generated by multiplying one multiplier bit with multiplicand and the partial products are shifted and added accordingly. The operation involves shifting and adding process. Array method of partial products accumulation was proposed by C.R. Baugh, and Fig. 2: Multiplication Steps

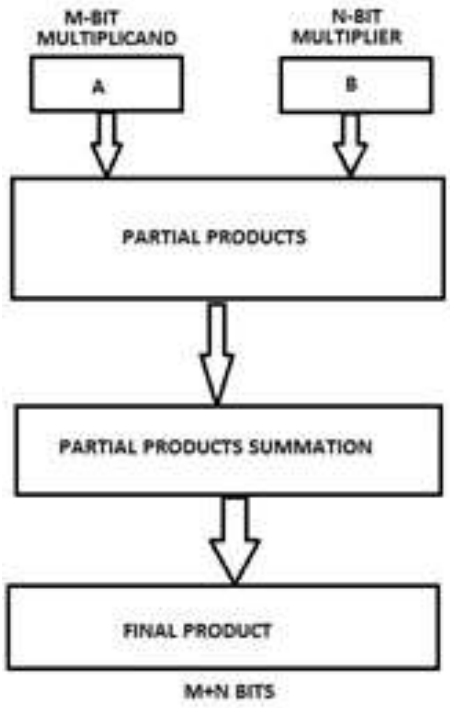

Fig. 1: Multiplication Steps

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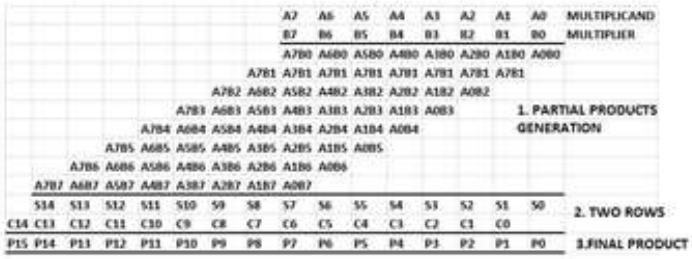

Fig. 2: Multiplication Steps

B.A. Wooley [18], P.E. Blankenship [19]. Array multipliers are suited best for faster computations in digital signal processing applications since it has simple interconnections. An array multiplier to perform multiplication of nxn bits requires n^2 no of AND gates and n(n-1) adders. The Figure 5 shows 4x4 Array Multiplier. Array Multiplier is easy to design and it is very slow due to large critical path.

Carry save Array Multiplier

Carry Save Array Multiplier uses Carry Save Adders to reduce the critical path delay. Carry Propagation Adder is used in the final stage for generation the final product. The Figure 6 shows 4x4 Carry Save Array Multiplier.

Wallace Tree Multiplier

Wallace Tree Multiplier was proposed in the year 1964 by C.S. Wallace [3]. It is fast method of performing multiplication. The performance of Wallace Tree Multiplier is faster for larger operands. The partial product matrix of an Array Multiplier is rearranged to form a tree like structure as shown in the figure. This reduces the number of adders and the critical path. Wallace Tree Multiplier uses column compression technique. Wallace tree has complexity in design. There are (2:2),(3:2),(4:2) and (5:2) compressors.

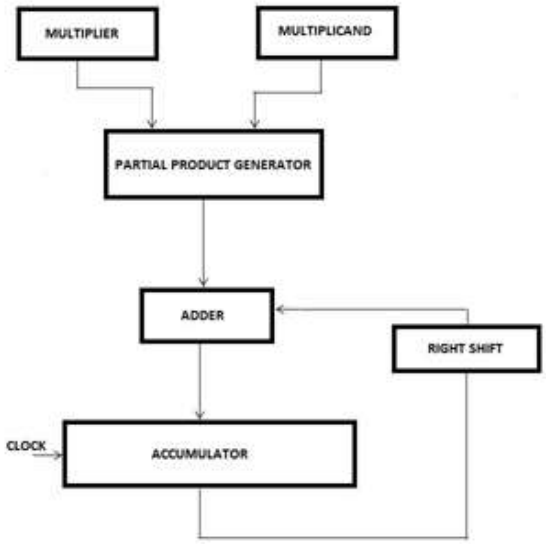

Fig. 3: Serial Multiplier

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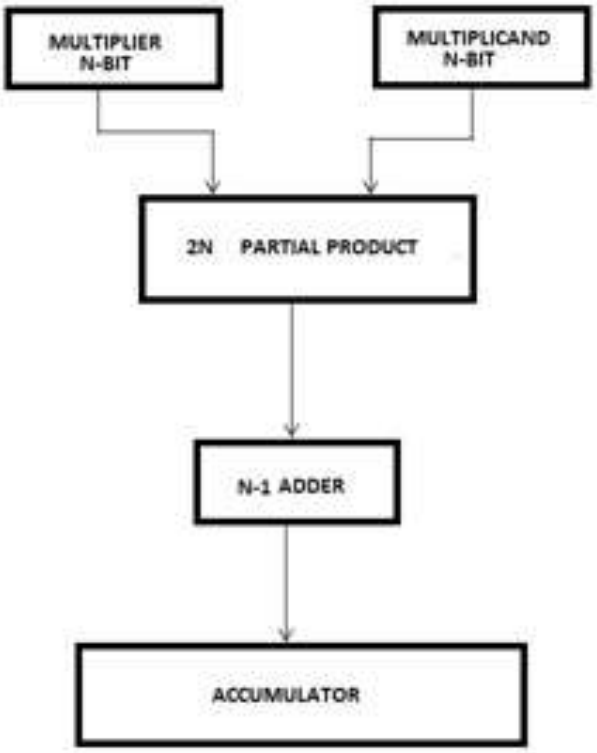

Fig. 4: Parallel Multiplier

The Figure Fig. 4: Parallel Multiplier 7 shows 8 bit Wallace Tree Multiplier using 3:2 compressor.

A. 2:2 Compressors

A Half adder is (2:2) compressor it takes two bits from a column of partial product matrix and produces two bits of output, one bit to the next column and one bit to the same column. The Figure 8 shows (2:2) compressor.

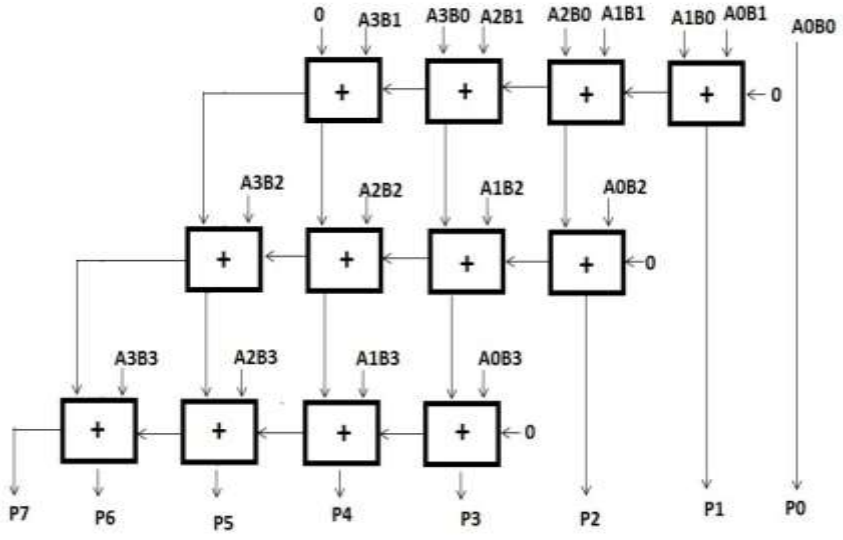

Fig. 5: Array Multiplier

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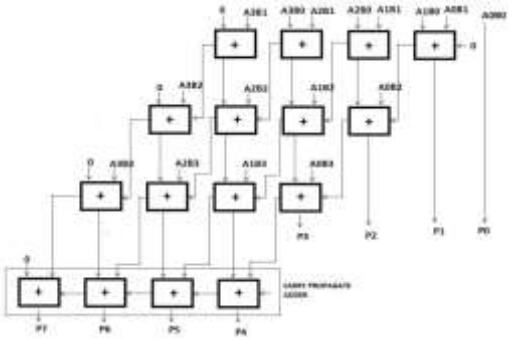

Fig. 6: Carry save Array Multiplier

B. 3:2 Compressors

Wallace Tree can use 3:2 Compressors proposed in Ahmed M. Shams, Tarek K. Darwish et al. [20] , Hung Tine Bui, Yuke Wang et al. [21]. A Full adder is (3:2) compressor it takes three bits from a column of partial product matrix and produces two bits of output , one bit to the next column and one bit to the same column. The Figure 9 shows (3:2) compressor.

Braun Multiplier

Braun Array is simplest multiplier.The simplest parallel multiplier is the Braun array. All the partial products are computed in parallel, then collected through a cascade of Carry Save Adders. The completion time is limited by the depth of the carry save array, and by the carry propagation in the adder. Note that this multiplier is only suited for positive operands. The structure of the Braun algorithm for the unsigned binary multiplication is shown in Figure 10

Vedic Multiplier

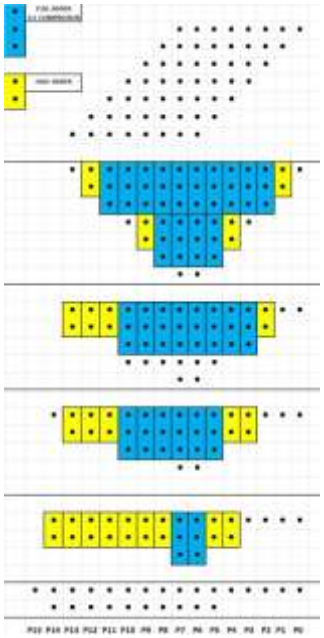

Fig. 7: Wallace Tree Multiplier using 3:2 Compressor

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Vedic Mathematics is ancient Indian system of Maths. The Vedic Maths is based on vedic sutras and there are 16 Vedic sutras. These 16 Vedic sutras describe the way of solving the problems mathematically. Vedic mathematics algorithms has been used in multiplication process of 8085 and 8086 microprocessors and there has been good time savings in the process. Vedic Multipliers can be used for high speed and low power applications and has less complexity as compared to that of a booth multiplier. Vedic multiplier also requires less hardware and hence the area is also less. Therefore Vedic Multipliers has advantages in terms of speed, area, complexity and power. Out of 16 sutras we use Urdhva triyagbhyam sutra technique for multiplication.

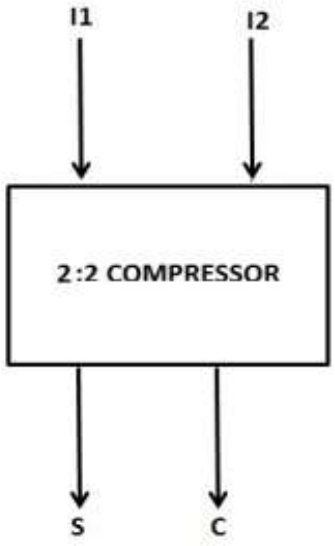

Fig. 8: 2:2 Compressor

The Figure 11 shows 2 X 2 multiplication process.

The Figure 12 shows 4 X 4 multiplication process.

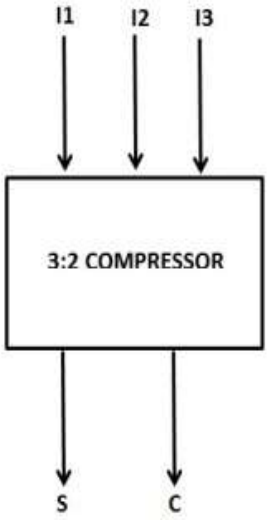

Fig. 9: 3:2 Compressor

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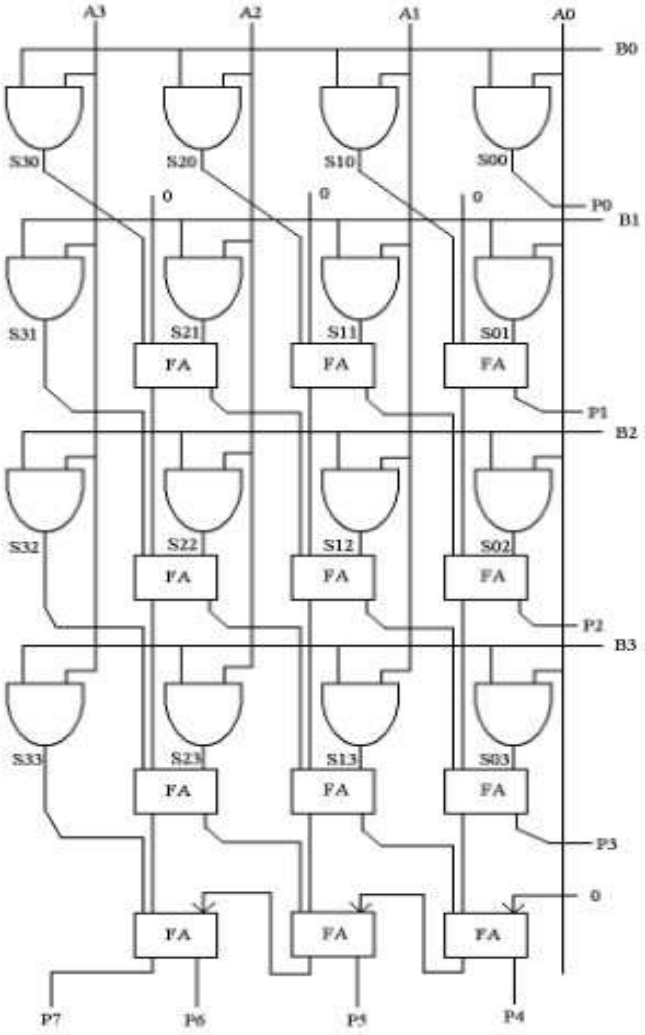

Fig. 10: Braun Multiplier

II. METHODOLOGY

Multipliers are designed using verilog coding. Full adder is designed using verilog gate primitives and using these Full Adders Array Multiplier is designed.In the same manner Carry Save Array Multiplier, Wallace Tree Multiplier, Braun Multiplier, Vedic Multiplier are designed. The designed multipliers are sythesized using Xilinx tool to find the power, time delay and area.

III. RESULTS

8-bit Array Multiplier, Wallace Tree Multiplier, Braun Multiplier, Carry save Multiplier and Vedic Multiplier has been simulated and synthesized using Xilinx ISE 9.1i. The Table 1 shows Area, Time delay and Power Consumption of Multipliers. The Figure 13 shows comparision of Area between the multipliers.The Figure 14 shows comparision of Time Delay between the multipliers.The Figure 15 shows comparision of Power consumption between the multipliers.

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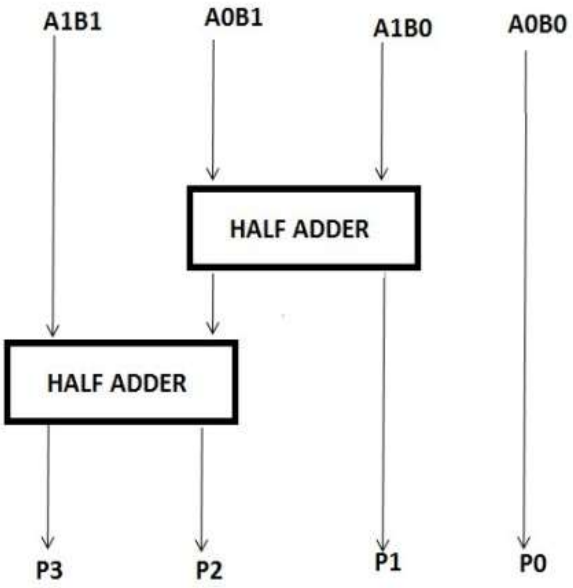

Fig. 11: Vedic 2x2 Multiplier

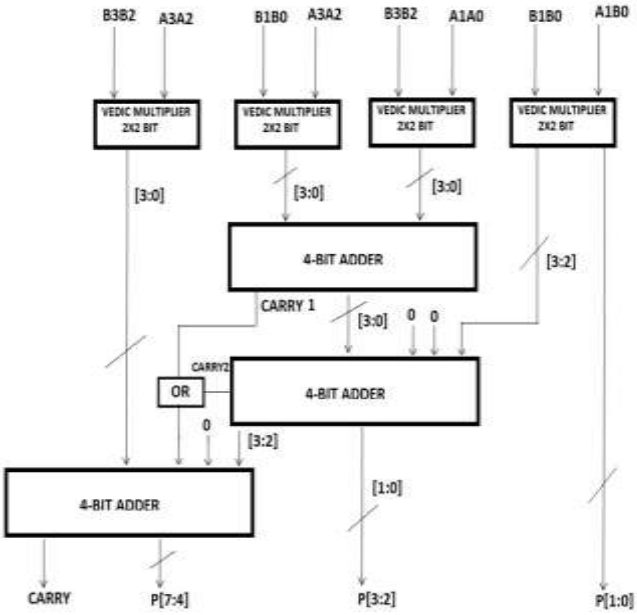

Fig. 12: Vedic 4x4 Multiplier

IV. CONCLUSION

The performance of Array Multiplier, Wallace Tree Multiplier, Braun Multiplier, Carry save Multiplier and Vedic Multiplier has been compared in terms of their speed, area and power and the results has shown that Wallace tree Multiplier has high speed and low power consumption compared with the other Multipiers. The power consumption of all the multipliers are same. The time delay wallace tree multiplier is low compared to other multipliers. Area of Array multiplier is low compared to the other multipliers.

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Table 1: Comparison of 8-Bit Multipliers

MULTIPLIER	NO LUT'S	OF	TIME DELAY(nS)	POWER CONSUMP-TION(mW)
Array Multiplier	73		3.849	73
Carry Save Array Multiplier	84		3.876	73
Wallace Tree Multiplier	89		3.749	73
Braun Multiplier	81		4.037	73
Vedic Multiplier	99		3.796	73

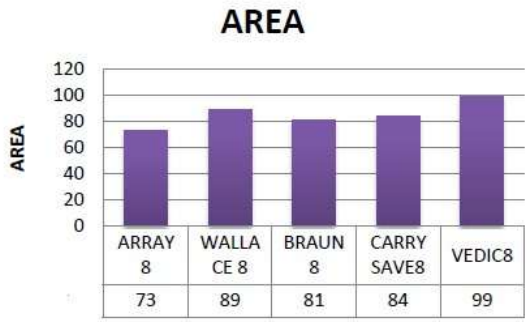

Fig. 13: Area

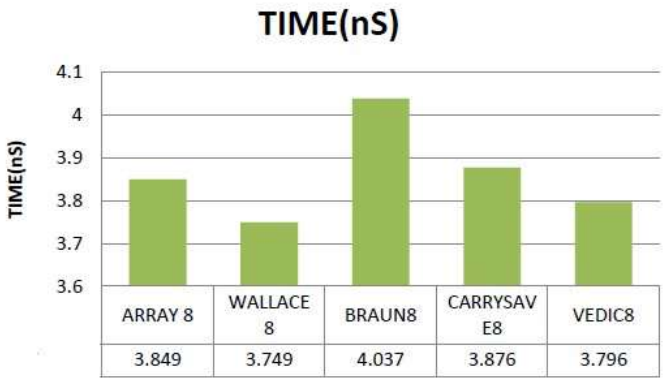

Fig. 14: Time Delay

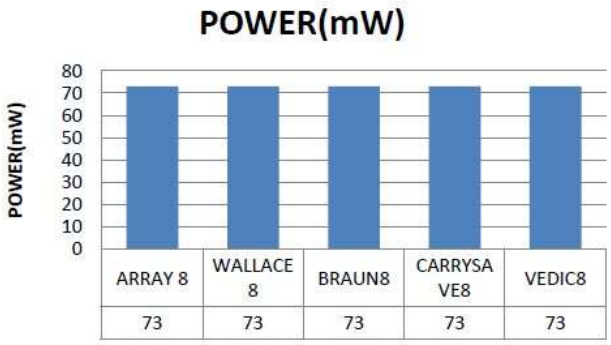

Fig. 15: Power

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