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Quasi-Floating Gate Based High Precision Current Mirror

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***Abstract*---** *Current mirror (CM) is a basic building block of several mixed signal circuits such as analog to digital converter, filter etc. The performance metrics of current mirror are its current transfer error ratio, input and output resistances, low input and output compliance voltages and bandwidth response. Out of these metric the current transfer error ratio is more significant parameter as it defines the accuracy of current copying capability in its dynamic range. Various topologies have been proposed with minimum current transfer error ratio. Such errors are greatly affected by the device mismatch governing of its construction parameters. The paper is targeted to achieve minimum current transfer error ratio at sub-volt supply. The proposed circuit uses a feedback loop from input to output and vice versa which enables it to compensate the error responsible of current mismatch. The design is simulated on 180nm node with the help of HSpice simulator.*

***Keywords*—** *Gate-Driven, Floating-gate, Quasi-floating gate, Current Mirror, Compliance voltage, Bandwidth, Power*

I INTRODUCTION

HE demand of portable electronic equipment has encouraged low voltage (LV) low power (LP) designs for both types of circuits i.e. analog and digital. The trend of technology down scaling and demand of low power requirements had put limitations on design of precise amplifiers with high gain, dynamic range and full signal swing. Nowadays IC designers are moving towards low power approaches [1], for example-Floating Gate Metal Oxide Semiconductor (FG-MOS) and Quasi Floating Gate Metal Oxide Semiconductor (QFG-MOS) transistors. Circuits based on FG MOS transistors can operate at much lower supply than conventional CMOS. The advantage of these devices lies in terms of charge storing capability on its floating gate and in terms on linearity as the capacitor divider makes input signal attenuate which increases the linearity at the expense of increased input-referred noise.

Current mirror (CM) is a circuit whose function is to copy currents to various blocks in the circuit. A most common example can be found in biasing blocks for operational transconductance amplifier, op-amps, stabilization, current amplification, active loading and level shifting [2]. The important parameters governing the current mirrors are accuracy, input/output compliances voltage limits, small signal input/output impedances, bandwidth, input/output curve (transfer characteristics). Many high performance and precise applications require an accurate current mirror [3, 4]. The simple current mirror unfit due to its degraded parameters like low output resistance and high current transfer error. The errors (mainly due to mismatch) deteriorate the performance of precise analog circuits mainly for short channel devices. It causes an unavoidable offset in output current. Various

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approaches [2] have been proposed to overcome such offset current and maintain accuracy at the expense of circuit's complexity. The accuracy of a current mirror is governed by the device electrical parameters. The closer the parameters, the better the accuracy of the output current produced. However, the perfect matching of transistors only exists in the world of fantasy. So, it is instructive to investigate various sources of mismatch and its effect on the performance of a current mirror which can be either deterministic (VDS mismatch) or random (Tran conductance & threshold voltage). However, the prominent mismatch is deterministic which can be overcome by careful design. It is very important to consider VDS mismatch as it greatly affects the accuracy of output current. The VDS mismatch effect is visible by presence of finite output impedance. The effect in the output current is due to channel length modulation. Through cascading and gain boosting techniques these mismatch can be compensated. In [5, 6] the current mirror was implemented using bulk-driven mechanism. This made CM immune to threshold voltage limitation and maximizes the input voltage swing. Further for current transfer accuracy, they implemented a feedback along with gate-driven cascade structure for extending the operating range of CM. For bandwidth enhancement, the architecture uses the resistive compensation scheme. Many modifications have been performed on this architecture to make it operable at low supply range. Some focused on achieving very low input and high output impedance by double-nested shunt feedback loop along with flipped voltage follower (FVF) architecture [7, 8]. To enhance bandwidth, the resistive compensation was used on self-cascode [9] as this structure requires the minimum input supply voltage. While [10] uses the feedback loop at the output node which decreases the compliance voltage with an appreciable increase of bandwidth. The way to proceed towards low power at minimum supply not only make circuits complex but also degrade some of its metrics.

Instead of approaching with complex circuitry, the MOS transistor is replaced by the well known architectures referred as FGMOS and QFGMOS. Use of such devices offers a floating node which helped in minimizing matching errors. Some of FGMOS based LV CM circuits can be found in [11-14]. These devices helped in designing CM [11, 12] with highly current matching and low voltage operation through applying potential on secondary terminal. Based on FGMOS, an op-amp [13, 14] was proposed where they perform direct implementation of linear weighted addition of continuous-time signals. Other applications like divider, voltage-controlled resistor, transresistance amplifier based on FGMOS were also proposed [15, 16]. With the advent of QFGMOS, nowadays the power consuming sections of standard circuits is replaced by QFGMOS transistors. A numerous examples can be found in implementation of LV mixers & switches [17, 18] op-amp [19] resistor [20] etc. It also gained interest in CM circuits as these circuits require high accuracy rate. Since QFGMOS is capable of processing signal from very low to high frequency, requirement of high bandwidth (BW) CM circuits were accomplished using QFGMOS [21-32]. In this work, a QFGMOS based current mirror is proposed with minimum current transfer error at high bandwidth. The paper is divided in five sections. Section II covers the basics on FGMOS and QFGMOS architectures followed by proposed CM circuit in section III. The simulation results are discussed in section IV and finally paper is concluded section V.

II PRELIMINARIES

II.I. Floating Gate MOSFET

The architecture of two-input N-type FGMOS with its parasitic capacitances is shown in Fig. 1.

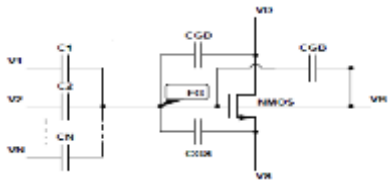

Fig.1. Two-input FGMOS transistor Equivalent circuit

The gate is at floating potential under DC condition whereas it is capacitive connected to input via second layer of ploy silicon. The input capacitor (C_1, C_2) formed is referred as poly-poly (PIP) capacitor while others (C_{GS}, C_{GD}, C_{GB}) are the parasitic capacitance associated the floating gate

node. Using the law of charge conservation at floating node potential (V_{FG}) , the calculated floating gate voltage is given as

$$V_{FG} = \frac{1}{C_T}\left(\sum_{k=1}^{N} C_k V_k + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B + Q_0\right) \quad (1)$$

where $C_T = C_1 + C_2 + ... + C_N + C_{GS} + C_{GD} + C_{GB}$, and Q_0 is the initial charge trapped in the floating gate during fabrication. Two issues were observed while working with FGMOS. The first issue was regarding initial charge trapping at FG node. Such charge trapping at floating node causes large DC offsets. The very common technique used for initial charge removal in FGMOS EPROM is Ultra Violet (UV) radiation. As the process of charge removal is done after fabrication. Since the process is costly, the analog designers were not involved much with such architectures in the past. Various techniques of charge removal were proposed which do not require any UV exposure [33]. They adopted the layout based approach for removal of initial charges from FG node. The second issue was regarding effective gate voltage at FG node. Due to capacitive voltage divider, the FG experiences an effective voltage less than the desired input. So, appropriate selection of capacitor became a tedious task for IC designers.

II.II. Quasi-floating Gate MOSFET

As discussed the FGMOS transistor has certain advantages but also suffers some of disadvantage. The scaling issue of input voltage in FGMOS was removed by using a large capacitance (C_{large}) ratio at FG node which forces the FG potential close to the supply rail. But such large coupling capacitor resulted in increased silicon area, notable reduced gain-bandwidth (GB) product in differential amplifier. To solve the issue, the researchers proposed architecture very much similar to FGMOS and named it as Quasi FGMOS (QFGMOS) transistor. They used a large value resistor as a replacement of capacitor (C_{large}) which they implemented using leakage resistance (R_{large}) of a reverse biased junction of MOS transistor operating in cut-off region. Through such large resistance they were able to connect the FG weakly to the desired DC level. The architecture of two-input N-channel QFGMOS is shown in Fig. 2.

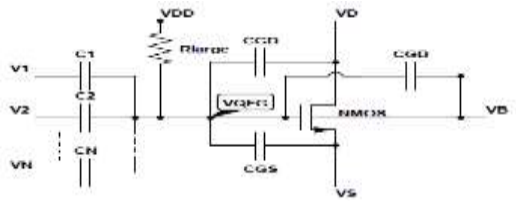

Fig.2. Two-input QFGMOS transistor equivalent circuit

The architecture is similar to FGMOS but here the quasi floating gate is set to the dc gate voltage V_B independently of the DC levels of the input voltages V_1 and V_2 . The effective quasi floating gate voltage under ac input in s-domain is expressed as

$$V_{QFG} = \frac{sR_{large}}{1+sR_{large}C_T^{'}}\left(\sum_{k=1}^{N} C_k V_k + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B\right) \qquad (2)$$

where $C_T = C_1 + C_2 + ... + C_N + C_{GS} + C_{GD} + C_{GB} + C_{GD}^{'}$ is the total capacitance and $C_{GD}^{'}$ is the parasitic capacitance of p-channel MOS transistor in cut-off region seen from gate. From the above equation, it is quite clear that the device is operating as high pass filter with its cut-off frequency of $\left(1/2\pi R_{large}C_T^{'}\right)$. Depending on the value of R_{large} the cut-off frequency can be made very low (less than 1 Hz). So, it can perform as weighted average of ac input voltages from very low frequency to high frequency without affecting the required results till it remains large enough.

III PROPOSED CURRENT MIRROR

In this paper, an approach to make equal VDS drop of MN1 and MN2 in QFGMOS CM is proposed. The proposed CM consists of a feedback loop as shown in Fig. 3. The loop enables both the transistors MN1 and MN2 to experience the same gate voltage and same VDS drop which make it to satisfy the basic necessary condition of accurate mirroring. The nested feedback loop increases the performance of the current copying without using complex circuitry.

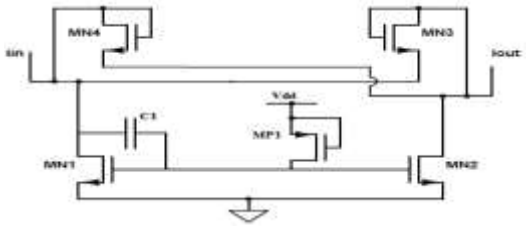

Fig.3. Proposed QFGMOS CM

For any MOS transistor, the condition for linear region is when drain-to-source voltage (V_{DS}) becomes lower than the overdrive voltage $(V_{GS} - V_{th})$. Under constant V_{GS} , the channel length modulation causes significant reduction in transistor output resistance which shows the dependency of drain-to-source current (I_{DS}) on V_{DS} variations. For MOS in saturation the drain current for N-channel is given as

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS}-V_{th}\right)^2\left(1+\lambda V_{DS}\right) \quad (3)$$

From (1), it is clear that if V_{GS} kept constant whereas V_{DS} has variations then it will affect I_{DS} . If somehow the variations in V_{DS} can be compensated through some feedback loop to the desired value of V_{DS} then the accuracy can be guaranteed for any value of current. The MN1 transistor act as input whereas MN2 as output transistor. The input signal is coupled via input capacitors C_1 and C_2 of MOSFETs MN1 and MN2. This QFG node is weakly connected to supply via high value resistor of MP working in cut-off region. The very common factor influencing signal swing is the threshold voltage of MOSFET. For a current mirror the dependence of input voltage on threshold voltage of input transistor puts the limitation on range of input compliance voltage. Using level shifter techniques [3], further reduction of input compliance can be easily achieved without affecting the circuit's frequency response. In fig. 3 the PMOS transistor MP1 acts as a level shifter which varies the drain potential of input transistor MN1 hence affecting the input compliance voltage range. The magnitude of I_{bias} determines the operating region of MP1 whereas MN1 depends on magnitude of both I_{bias} and I_{in} .The most desired operating mode for MP1 is cut-off region which results in high impedance and do not disturb the input-output impedances of CM.

The condition for exact current copy is to have $V_{GS1}=V_{GS2}$ and $V_{DS1}=V_{DS2}$ .Though it can be assured that $V_{GS1}=V_{GS2}=V_{QFG}$ but V_{DS1} cannot be guaranteed to be equal to V_{DS2} . So, the goal is to achieve $V_{DS1}=V_{DS2}$. There can be either of two cases:

Case (i) when $V_{DS1}<V_{DS2}$, under this case add an extra correction factor of V_{C1} which will make $V_{DS1}=V_{DS2}$

i.e. $V_{C1}=V_{DS2}-V_{DS1}$ (4)

Case (ii) when $V_{DS1}>V_{DS2}$, under this case again add an extra correction factor of V_{C2} which will make

$V_{C2}=V_{DS1}-V_{DS2}$

From (4) & (5), it can be observed that to hold the condition $V_{DS1}=V_{DS2}$ true, the value of correction factors is to be made such that it satisfies the two conditions: $V_{C1}\&V_{C2}$ are equal and $V_{C1}\&V_{C2}$ are out of phase. The proposed CM architecture replaces the correction factor V_{C1} and V_{C2} with V_{GS3} and V_{GS4} of the diode connected MOS transistor MN3 & MN4 respectively. The input voltage get added up with V_{GS3} whereas the output with V_{GS4} , and the resulting new voltage appearing at input & output terminals are

$V_{in}=V_{DS1}+V_{GS3}$ (6)

$V_{in}=V_{DS1}+V_{DS2}-V_{DS1}=V_{DS2}$ (7)

$V_{out}=V_{DS2}+V_{GS4}$ (8)

$$V_{out} = V_{DS2} + V_{DS1} - V_{DS2} = V_{DS1} \quad (9)$$

$$\text{Also, } V_{GS3} = -\left(V_{GS4}\right) \quad (10)$$

From (7) & (9), the voltages reflection with equal amplitude can be seen which fulfills the first desired condition whereas (10) fulfills the second desired condition. Also

$$V_{DS2} = V_{GS3} + V_{DS1} \quad (11)$$

$$V_{GS3} = V_{DS2} - V_{DS1} \quad (12)$$

$$V_{DS1} = V_{GS4} + V_{DS2} \quad (13)$$

$$V_{GS4} = V_{DS1} - V_{DS2} \quad (14)$$

When the input current ranges from low to high value, the input & output device remains in saturation mode due to the charge developed by pull up resistor (MP) whereas there is variation in their respective V_{DS} . Under the case, when $V_{DS1} < V_{DS2}$ then (12) becomes positive which force MN3 to be in saturation mode whereas (14) becomes negative which makes MN4 in cut-off mode. This difference of voltage is compensated with the feedback which raises the input voltage to be equal to output voltage. Similarly, for the case when $V_{DS1} > V_{DS2}$ then (12) becomes negative which force MN3 to be in cut-off mode whereas (14) becomes positive which makes MN4 in saturation mode and the feedback raises the output voltage to be equal to input voltage $\left(V_{DS1} = V_{DS2}\right)$. The drain-to-source current $\left(I_{DS}\right)$ for MN1, MN2, MN3, & MN4 in saturation mode is given as

$$I_{DS1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \left(V_{QFG} - V_{th}\right)^2 \quad (15)$$

$$I_{DS2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left(V_{QFG} - V_{th}\right)^2 \quad (16)$$

$$I_{DS3} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 \left(\left(V_{DS2} - V_{DS1}\right) - V_{th}\right)^2 \quad (17)$$

$$I_{DS4} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_4 \left(\left(V_{DS1} - V_{DS2}\right) - V_{th}\right)^2 \quad (18)$$

From Fig. 6,

$$I_{DS1} = I_{in} + I_{DS3} - I_{DS4} \quad (19)$$

$$I_{in} = I_{DS1} + \left(I_{DS4} - I_{DS3}\right) \quad (20)$$

$$I_{DS2} = I_{out} + I_{DS4} - I_{DS3} \quad (21)$$

$$I_{out} = I_{DS2} - \left(I_{DS4} - I_{DS3}\right) \quad (22)$$

Under assumption of no channel length modulation, and each transistor having identical aspect ratio $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$ then

$$I_{DS4} - I_{DS3} = k\left(V_{DS1} - V_{DS2} - V_{th}\right)^2 - k\left(V_{DS2} - V_{DS1} - V_{th}\right)^2 \quad (23)$$

Solving, $\left(V_{DS1} = V_{DS2}\right)$

$$I_{DS4} - I_{DS3} = 4kV_{th}\left(V_{DS2} - V_{DS1}\right) \quad (24)$$

Putting (24) in (20) & (22),

$$I_{in} = k\left(V_{QFG} - V_{th}\right)^2 + 4kV_{th}(V_{DS2} - V_{DS1}) \quad (25)$$

$$I_{out} = k\left(V_{QFG} - V_{th}\right)^2 - 4kV_{th}(V_{DS2} - V_{DS1}) \quad (26)$$

Solving (25) & (26)

$$I_{in} - I_{out} = 8kV_{th}\left(V_{DS2} - V_{DS1}\right) \quad (27)$$

Using nodal analysis on input & output terminals of Fig. 3 and solving for $\left(I_{in} - I_{out}\right)$,

$$I_{in} - I_{out} = \frac{V_{DS1}}{r_{ds1}} - \frac{V_{DS2}}{r_{ds2}} \quad (28)$$

Equalizing (27) and (28),

$$8kV_{th}\left(V_{DS2} - V_{DS1}\right) = \frac{V_{DS1}}{r_{ds1}} - \frac{V_{DS2}}{r_{ds2}} \quad (29)$$

$$\left(\frac{1}{r_{ds1}} + 8kV_{th}\right)V_{DS1} = \left(\frac{1}{r_{ds2}} + 8kV_{th}\right)V_{DS2} \quad (30)$$

Since $8kV_{th} << \frac{1}{r_{ds1,2}}$

$$V_{DS1} = V_{DS2} \quad (31)$$

Hence, the desired condition of accuracy is achieved. This relation holds true for high value to current range. For example, in this paper the simulation has been performed to 500 micro amperes range which can be further validated for milli amperes range. The frequency analysis of proposed mirror is shown in Fig. 4. Here, the transistors are assumed to be in saturation region having infinite small-signal output resistance. Since, MP1 is in cut-off region, the parasitic capacitances associated are neglected.

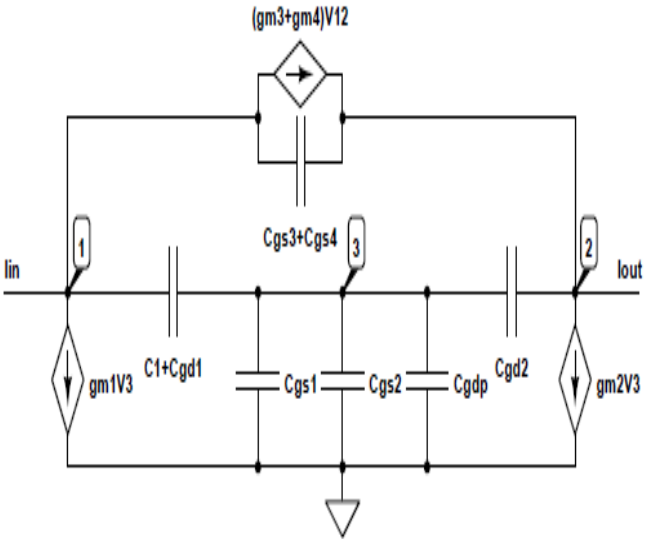

Fig 4. High frequency model of Proposed CM

$$I_{in} = g_{m1}V_3 + s\left(C_{gd1} + C_1\right)V_{13} + \left(g_{m3} + g_{m4}\right)V_{12} + s\left(C_{gs3} + C_{gs4}\right)V_{12} \quad (32)$$

$$I_{out} = g_{m2}V_3 + sC_{gd2}V_{23} - \left(g_{m3} + g_{m4}\right)V_{12} - s\left(C_{gs3} + C_{gs4}\right)V_{12} \quad (33)$$

Let $I_x = \left(\left(g_{m3} + g_{m4}\right) + s\left(C_{gs3} + C_{gs4}\right)\right)V_{12}$ then

$$I_{in} = g_{m1}V_3 + s\left(C_{gd1} + C_1\right)V_{13} + I_x \quad (34)$$

$$I_{out} = g_{m2}V_3 + sC_{gd2}V_{23} - I_x \quad (35)$$

Also, applying nodal analysis at node 3,

$$s\left(C_{gs1} + C_{gs2} + C_{gdp}\right)V_3 + sC_{gd2}V_{32} + s\left(C_{gd1} + C_1\right)V_{31} = 0 \quad (36)$$

$$s\left(C_{gd1} + C_1\right)V_{13} + sC_{gd2}V_{23} = s\left(C_{gs1} + C_{gs2} + C_{gdp}\right)V_3 \quad (37)$$

$$I_{in} + I_{out} = g_{m1}V_3 + s\left(C_{gd1} + C_1\right)V_{13} + g_{m2}V_3 + sC_{gd2}V_{23} \quad (38)$$

$$I_{in} + I_{out} = g_{m1}V_3 + g_{m2}V_3 + s\left(C_{gs1} + C_{gs2} + C_{gdp}\right)V_3 \quad (39)$$

$$V_3 = \frac{I_{in} + I_{out}}{\left(g_{m1} + g_{m2}\right) + s\left(C_{gs1} + C_{gs2} + C_{gdp}\right)} \quad (40)$$

From (34) as I_{in} increases by I_x , there is corresponding decrease in I_{out} by I_x but as these variations do not affect (40) the output current keep tracking input current.

IV SIMULATION RESULTS

The proposed CM circuit simulation is carried out using 0.18 micron technology, BSIM3, Level 49 with the help of HSpice simulator. The current mirror runs on single volt supply of 0.5V. The accuracy of circuit is verified for 0 to 1000 μA range. The W/L ration of each transistor is shown in table 1.

Table 1: W and L of MOS transistors in proposed CM

Transistor	W (μm)	L (μm)
MN1	20	0.24
MN2	20	0.24
MN3	0.24	0.24
MN4	0.24	0.24
MP	0.24	0.24
C1=1pf, Vdd=0.5V		

The transfer characteristic (I_{out}/I_{in}) under input as DC current from 0 to 1000uA is shown in Fig. 5 and the current transfer error is shown in Fig. 6. From both the figures it can be observed that the error in current transfer is minimum for the proposed current mirror compared to simple current mirror. The frequency response in shown in Fig. 7, where the bandwidth observed by proposed current mirror is 600MHz whereas the simple current mirror has 700MHz.

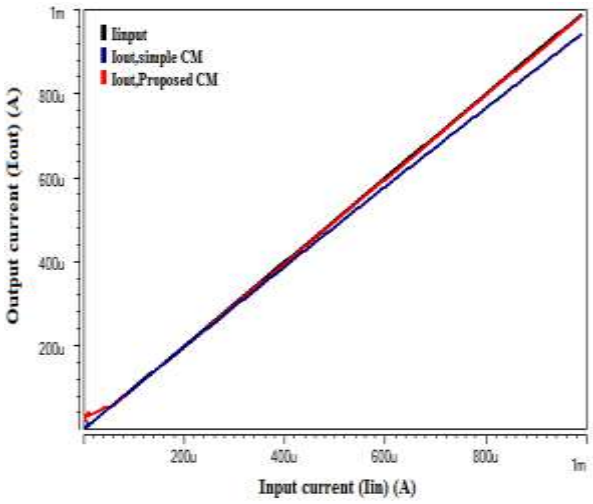

Fig.5. Current transfer characteristics

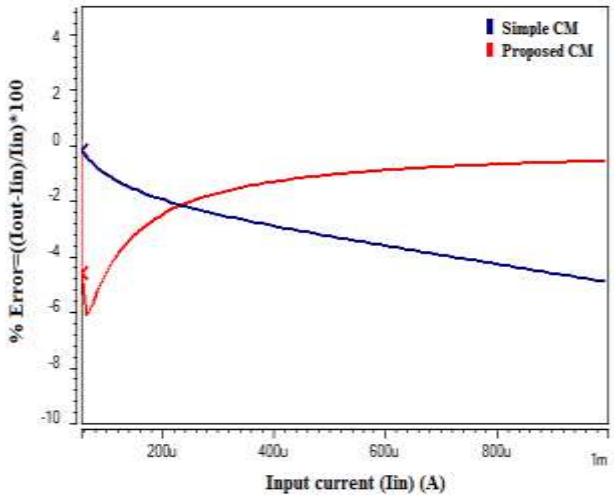

Fig.6: Error in current transfer characteristics

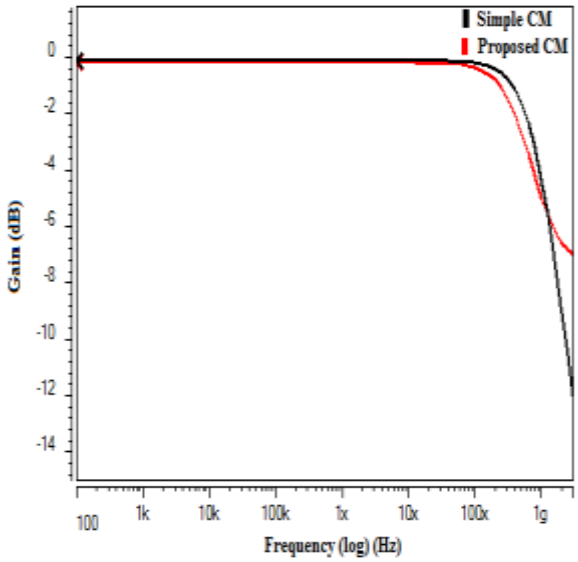

Fig. 7. Frequency response

V CONCLUSION

Use of FGMOS and QFGMOS devices can be beneficial to improve performance in CMOS current mirror for LV architectures. A novel wide bandwidth low power QFGMOS current mirror has been proposed in this paper. The circuit features high current driving capability maintaining high accuracy for high input current. The frequency response of proposed CM can be made even much better using the resistive compensation technique. The circuit has been implemented using 0.18 twin-well process through HSpice simulator.

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